Datasheet

APM32E103VET6S

Arm® Cortex®-M3 based 32-bit MCU

Version: V1.5

1. Product characteristics

- **Core**
  - 32-bit Arm® Cortex®-M3 core
  - Up to 96MHz working frequency
- **Memory**
  - Flash：512KB
  - SRAM：128KB
  - EMMC: Supports CF card, SRAM, PSRAM, SDRAM NOR and NAND memory
  - SDRAM：2MB
- **Clock**
  - HSECLK: 4~16MHz external crystal/ceramic oscillator supported
  - LSECLK: 32.768KHz crystal/ceramic oscillator supported
  - HSICLK: 8MHz RC oscillator calibrated by factory
  - PLL: Phase locked loop, 2~16 times of frequency supported
- **Reset and power management**
  - V_{DD} range: 2.0～3.6V
  - V_{DDA} range: 2.0～3.6V
  - V_{BAT} range of backup domain power supply: 1.8V～3.6V
  - Power-on/power-down reset (POR/PDR) supported
  - Programmable power supply voltage detector supported(PVD)
- **Low-power mode**
  - Sleep, stop and standby modes supported
- **DMA**
  - Two DMA; DMA1 supports 7 channels and DMA2 supports 5 channels
- **Debugging interface**
  - JTAG
  - SWD
- **I/O**
  - Up to 55 I/Os
  - All I/Os can be mapped to external interrup vector
  - Up to 39 FT input I/Os
- **Communication peripherals**
  - 1 I2C interfaces (1Mbit/s), support SMBus/PMBus
  - 3 USART, support ISO7816, LIN and IrDA functions
  - 3 SPI (18Mbps) interfaces, two of which support I2S interface multiplexing
  - 2 CAN, USBD and CAN can work independently at the same time
  - 1 USBD
- **Analog peripherals**
  - 3 12-bit ADCs
  - 2 12-bit DACs
- **Timer**
  - 2 16-bit advanced timers TMR1/8 that can provide 7-channel PWM output, support dead zone generation and braking input functions
  - 4 16-bit general-purpose timers TMR2/3/4/5, each with up to 4 independent channels to support input capture, output comparison, PWM, pulse count and other functions
  - 2 16-bit basic timers TMR6/7
  - 2 watchdog timers: one independent watchdog IWDT and one window watchdog WWDT
  - 1 24-bit autodecrement SysTick Timer
- **RTC**
  - Support calendar and clock functions
- **84Bytes backup register**
- **FPU**
- **CRC computing unit**
- **96-bit unique device ID**

Catalog

2. Product information

See the following table for APM32E103VET6S product functions and peripheral configuration.

Table 1 Functions and Peripherals of APM32E103VET6S Chip

产品		**APM32E103VE**
Model		APM32E103VET6S
Package		LQFP100
Core and maximum working frequency		Arm® 32-bit Cortex®-M3@96MHz
Operating voltage		2.0~3.6V(1)
Flash(KB)		512
SRAM(KB)		128
SDRAM(MB)		2
GPIOs		55
Communication interface	USART	3
	SPI/I2S	3/2
	I2C	1
	I2C3	1
	USBD	1
	CAN	2
Timer	16-bit advanced	2
	16-bit general	4
	16-bit basic	2
	System tick timer	1
	Watchdog	2
Real-time clock		1
12-bit ADC	Unit	3
	External channel	16
	Internal channel	2
12-bit DAC	Unit	2
	Channel	2
Operating temperature		Ambient temperature:-40℃~85℃ Junction temperature: -40℃~105℃

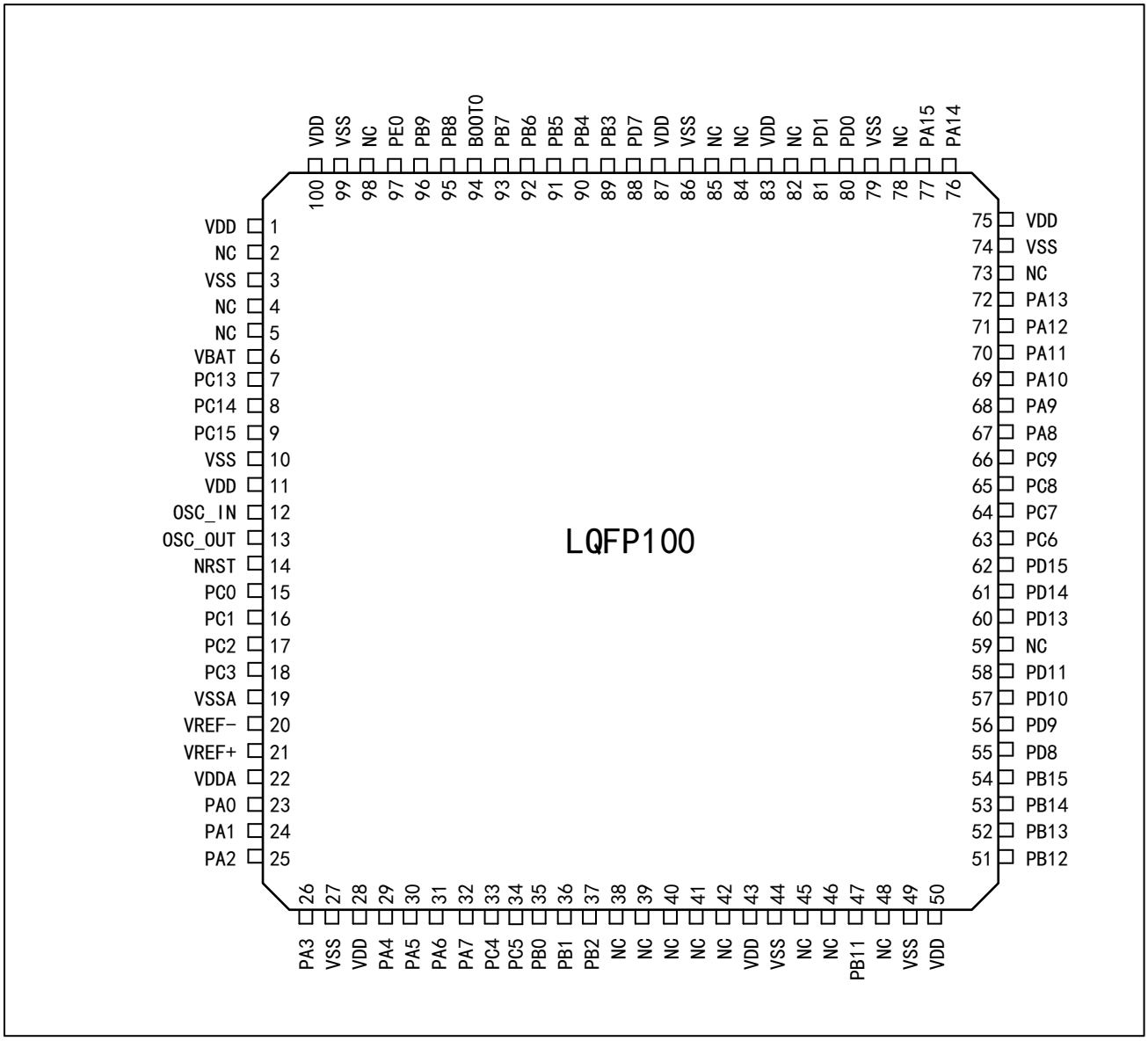
Note:

(1) When SDRAM is not used, the working voltage is 2.0V-3.6V; To use SDRAM, the operating voltage should be 3.0V - 3.6V.

3. Pin information

3.1. Pin distribution

Figure 1 Distribution Diagram of APM32E103VET6S LQFP100 Pins



Note: When using SDRAM, the PB11 pin must be not connected.

3.2. Pin function description

Table 2 Legends/Abbreviations Used in Output Pin Table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name	

Name		Abbreviation	Definition
Pin type		P	Power pin
		I	Only input pin
		I/O	I/O pin
I/O structure		5T	FT I/O
		5Tf	FT I/O, FM+ function
		STDA	I/O with 3.3 V standard, directly connected to ADC
		STD	I/O with 3.3 V standard
		B	Dedicated Boot0 pin
		RST	Bidirectional reset pin with built-in pull-up resistor
Note		Unless otherwise specified in the notes, all I/O is set as floating input during and after reset	
Pin function	Default multiplexing function	Function directly selected/enabled through peripheral register	
	Remap	Select this function through AFIO remapping register	

Table 3 Description of APM32E103VET6S by Pin Number

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	LQFP100
V_{DD}	P	-	-	-	1
NC	-	-	-	-	2
V_{SS}	P	-	-	-	3
NC	-	-	-	-	4
NC	-	-	-	-	5
V_{BAT}	P	-	-	-	6
PC13 (PC13)	I/O	STD	TAMPER-RTC	-	7
PC14 (PC14)	I/O	STD	OSC32_IN	-	8
PC15 (PC15)	I/O	STD	OSC32_OUT	-	9
V_{SS}	P	-	-	-	10
V_{DD}	P	-	-	-	11
OSC_IN	I	STD	-	PD0	12
OSC_OUT	O	STD	-	PD1	13
NRST	I/O	RST	-	-	14
PC0	I/O	STDA	ADC123_IN10	-	15

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	LQFP100
PC1	I/O	STDA	ADC123_IN11	-	16
PC2	I/O	STDA	ADC123_IN12	-	17
PC3	I/O	STDA	ADC123_IN13	-	18
V_{SSA}	P	-	-	-	19
V_{REF-}	P	-	-	-	20
V_{REF+}	P	-	-	-	21
V_{DDA}	P	-	-	-	22
PA0 (PA0)	I/O	STDA	WKUP, USART2_CTS, ADC123_IN0, TMR2_CH1_ETR, TMR5_CH1, TMR8_ETR	-	23
PA1	I/O	STDA	USART2_RTS, ADC123_IN1, TMR5_CH2, TMR2_CH2	-	24
PA2	I/O	STDA	USART2_TX, TMR5_CH3, ADC123_IN2, TMR2_CH3	-	25
PA3	I/O	STDA	USART2_RX, TMR5_CH4, ADC123_IN3, TMR2_CH4	-	26
V_{SS}	P	-	-	-	27
V_{DD}	P	-	-	-	28
PA4	I/O	STDA	SPI1_NSS, USART2_CK, DAC_OUT1, ADC12_IN4	-	29
PA5	I/O	STDA	SPI1_SCK, DAC_OUT2, ADC12_IN5	-	30
PA6	I/O	STDA	SPI1_MISO, TMR8_BKIN, ADC12_IN6 TMR3_CH1	TMR1_BKIN	31
PA7	I/O	STDA	SPI1_MOSI,	TMR1_CH1N	32

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	LQFP100
			TMR8_CH1N, ADC12_IN7, TMR3_CH2		
PC4	I/O	STDA	ADC12_IN14	-	33
PC5	I/O	STDA	ADC12_IN15	-	34
PB0	I/O	STDA	ADC12_IN8, TMR3_CH3, TMR8_CH2N	TMR1_CH2N	35
PB1	I/O	STDA	ADC12_IN9, TMR3_CH4, TMR8_CH3N	TMR1_CH3N	36
PB2 (PB2,BOOT1)	I/O	5T	-	-	37
NC	-	-	-	-	38
NC	-	-	-	-	39
NC	-	-	-	-	40
NC	-	-	-	-	41
NC	-	-	-	-	42
V_{DD}	P	-	-	-	43
V_{SS}	P	-	-	-	44
NC	-	-	-	-	45
NC	-	-	-	-	46
PB11	I/O	5T	I2C2_SDA, USART3_RX DMC_CKE	TMR2_CH4	47
NC	-	-	-	-	48
V_{SS}	P	-	-	-	49
V_{DD}	P	-	-	-	50
PB12	I/O	5T	SPI2_NSS, I2C2_SMBAI, I2S2_WS, USART3_CK, TMR1_BKIN, CAN2_RX	-	51
PB13	I/O	5T	SPI2_SCK, I2S2_CK, USART3_CTS,	-	52

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	LQFP100
			TMR1_CH1N, CAN2_TX		
PB14	I/O	5T	SPI2_MISO, TMR1_CH2N, USART3_RTS	-	53
PB15	I/O	5T	SPI2_MOSI, I2S2_SD, TMR1_CH3N	-	54
PD8	I/O	5T	-	USART3_TX	55
PD9	I/O	5T	-	USART3_RX	56
PD10	I/O	5T	-	USART3_CK	57
PD11	I/O	5T	-	USART3_CTS	58
NC	-	-	-	-	59
PD13	I/O	5T	SMC_A18	TMR4_CH2	60
PD14	I/O	5T	SMC_D0	TMR4_CH3	61
PD15	I/O	5T	SMC_D1	TMR4_CH4	62
PC6	I/O	5T	I2S2_MCK, TMR8_CH1	TMR3_CH1	63
PC7	I/O	5T	I2S3_MCK, TMR8_CH2	TMR3_CH2	64
PC8	I/O	5T	TMR8_CH3	TMR3_CH3	65
PC9	I/O	5T	TMR8_CH4	TMR3_CH4	66
PA8	I/O	5T	USART1_CK, TMR1_CH1, MCO	-	67
PA9	I/O	5T	USART1_TX, TMR1_CH2	-	68
PA10	I/O	5T	USART1_RX, TMR1_CH3	-	69
PA11	I/O	5T	USART1_CTS, USBD1DM, USBD2DM, CAN1_RX, TMR1_CH4	-	70
PA12	I/O	5T	USART1_RTS, USBD1DP USBD2DP, CAN1_TX, TMR1_ETR	-	71

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	LQFP100
PA13 (JTMS,SWDIO)	I/O	5T	-	-	72
NC	-	-	-	-	73
V_{SS}	P	-	-	-	74
V_{DD}	P	-	-	-	75
PA14 (JTCK,SWCLK)	I/O	5T	-	-	76
PA15 (JTDI)	I/O	5T	SPI3_NSS, I2S3_WS	TMR2_CH1_ETR, PA15, SPI1_NSS	77
NC	-	-	-	-	78
V_{SS}	P	-	-	-	79
PD0	I/O	5T	SMC_D2	CAN1_RX	80
PD1	I/O	5T	SMC_D3	CAN1_TX	81
NC	-	-	-	-	82
V_{DD}	P	-	-	-	83
NC	-	-	-	-	84
NC	-	-	-	-	85
V_{SS}	P	-	-	-	86
V_{DD}	P	-	-	-	87
PD7	I/O	5T	-	USART2_CK	88
PB3 (JTDO)	I/O	5T	SPI3_SCK, I2S3_CK	PB3, TRACESWO, TMR2_CH2, SPI1_SCK	89
PB4 (NJTRST)	I/O	5T	SPI3_MISO	PB4, TMR3_CH1, SPI1_MISO	90
PB5	I/O	STD	SPI3_MOSI, I2C1_SMBAI, I2S3_SD	TMR3_CH2, SPI1_MOSI, CAN2_RX	91
PB6	I/O	5T	I2C1_SCL, I2C3_SCL, TMR4_CH1	USART1_TX, CAN2_TX	92
PB7	I/O	5T	I2C1_SDA, I2C3_SDA, TMR4_CH2,	USART1_RX	93

Name (Function after reset)	Type	Structure	Default multiplexing function	Remap	LQFP100
			SMC_NADV		
BOOT0	I	B	-	-	94
PB8	I/O	5T	TMR4_CH3	I2C1_SCL, I2C3_SCL, CAN1_RX	95
PB9	I/O	5T	TMR4_CH4	I2C1_SDA, I2C3_SDA, CAN1_TX	96
PE0	I/O	5T	TMR4_ETR, SMC_NBL0	-	97
NC	-	-	-	-	98
V_{SS}	P	-	-	-	99
V_{DD}	P	-	-	-	100

Note:

(1) PC13, PC14 and PC15 are powered through the power switch. Since the switch only sinks limited current (3mA), the use of GPIO from PC13 to PC15 in output mode is limited:

① The speed shall not exceed 2MHz when the heavy load is 30pF;

② Not used for current source (e.g. driving LED).

(2)When using SDRAM, the PB11 pin must be not connected.

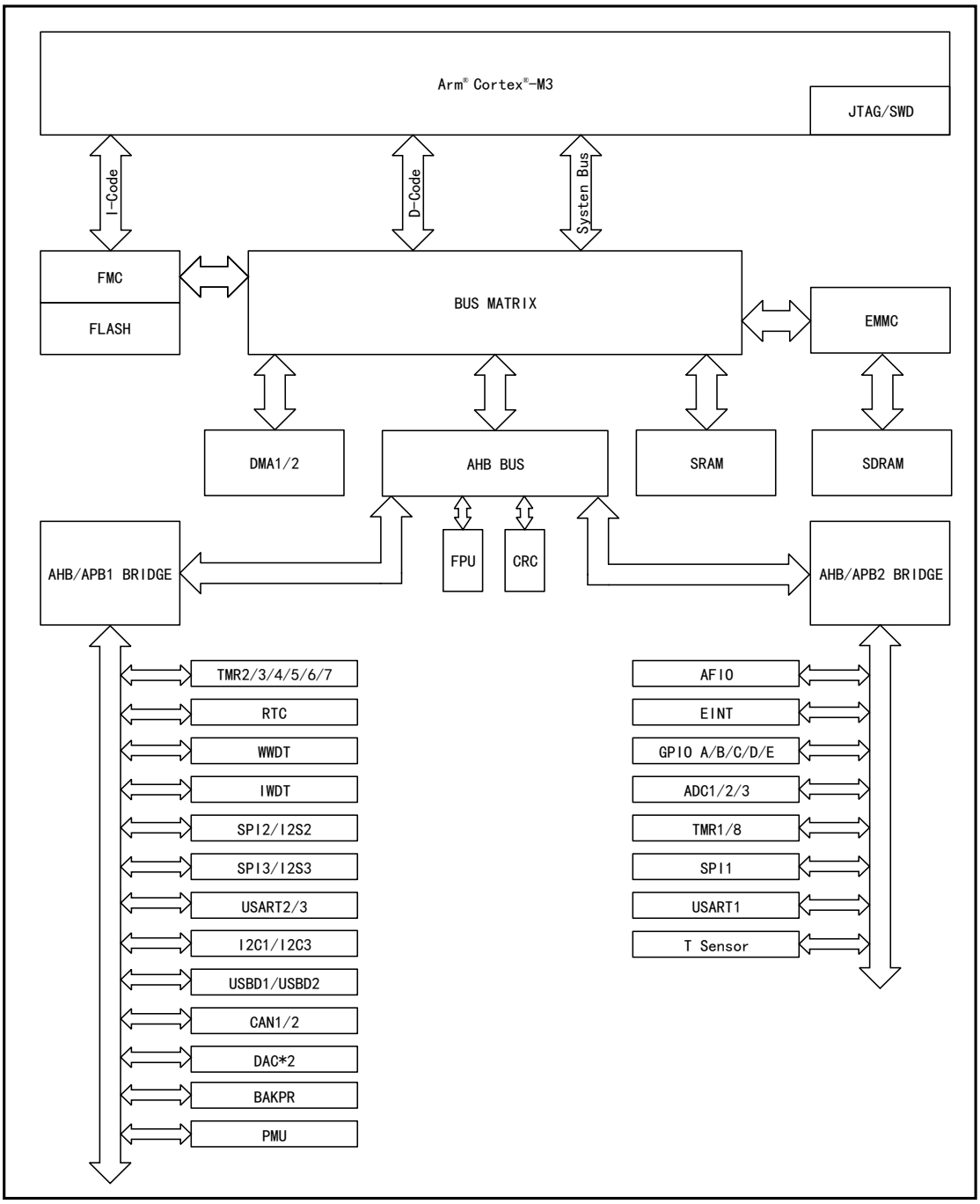
4. Functional description

This chapter mainly introduces the system architecture, interrupt, on-chip memory, clock, power supply and peripheral features of APM32E103VET6S; for information about the Arm® Cortex®-M3 core, please refer to the Arm® Cortex®-M3 technical reference manual, which can be downloaded from Arm's website.

4.1. System architecture

4.1.1. System block diagram

Figure 2APM32E103VET6S System Block Diagram



4.1.2. Address mapping

Table 4 APM32E103VET6S Performance Line Address Mapping Diagram

Region	Start Address	Peripheral Name
Code	0x0000 0000	Mapping area
Code	0x0800 0000	Flash
Code	0x0808 0000	Reserved
Code	0x1FFF F000	System Memory
Code	0x1FFF F800	Option Bytes
Code	0x1FFF F810	Reserved
SRAM	0x2000 0000	SRAM
APB1 bus	0x4000 0000	TMR2
APB1 bus	0x4000 0400	TMR3
APB1 bus	0x4000 0800	TMR4
APB1 bus	0x4000 0C00	TMR5
APB1 bus	0x4000 1000	TMR6
APB1 bus	0x4000 1400	TMR7
APB1 bus	0x4000 1800	Reserved
APB1 bus	0x4000 2800	RTC
APB1 bus	0x4000 2C00	WWDT
APB1 bus	0x4000 3000	IWDT
APB1 bus	0x4000 3400	Reserved
APB1 bus	0x4000 3800	SPI2/I2S2
APB1 bus	0x4000 3C00	SPI3/I2S3
APB1 bus	0x4000 4000	Reserved
APB1 bus	0x4000 4400	USART2
APB1 bus	0x4000 4800	USART3
APB1 bus	0x4000 4C00	Reserved
APB1 bus	0x4000 5000	Reserved
APB1 bus	0x4000 5400	I2C1(I2C3)
APB1 bus	0x4000 5800	Reserved
APB1 bus	0x4000 5C00	USBD1(USBD2)
APB1 bus	0x4000 6000	USBD/CAN SRAM
APB1 bus	0x4000 6400	CAN1
APB1 bus	0x4000 6800	CAN2

Region	Start Address	Peripheral Name
APB1 bus	0x4000 6C00	BAKPR
APB1 bus	0x4000 7000	PMU
APB1 bus	0x4000 7400	DAC
—	0x4000 7800	Reserved
APB2 bus	0x4001 0000	AFIO
APB2 bus	0x4001 0400	EINT
APB2 bus	0x4001 0800	Port A
APB2 bus	0x4001 0C00	Port B
APB2 bus	0x4001 1000	Port C
APB2 bus	0x4001 1400	Port D
APB2 bus	0x4001 1800	Port E
APB2 bus	0x4001 1C00	Reserved
APB2 bus	0x4001 2000	Reserved
APB2 bus	0x4001 2400	ADC1
APB2 bus	0x4001 2800	ADC2
APB2 bus	0x4001 2C00	TMR1
APB2 bus	0x4001 3000	SPI1
APB2 bus	0x4001 3400	TMR8
APB2 bus	0x4001 3800	USART1
APB2 bus	0x4001 3C00	ADC3
—	0x4001 4000	Reserved
AHB bus	0x4001 8000	Reserved
AHB bus	0x4001 8400	Reserved
AHB bus	0x4002 0000	DMA1
AHB bus	0x4002 0400	DMA2
AHB bus	0x4002 0400	Reserved
AHB bus	0x4002 1000	RCM
AHB bus	0x4002 1400	Reserved
AHB bus	0x4002 2000	Flash Interface
AHB bus	0x4002 2400	Reserved
AHB bus	0x4002 3000	CRC
AHB bus	0x4002 3400	Reserved
AHB bus	0x4002 4000	FPU

Region	Start Address	Peripheral Name
AHB bus	0x0002 4400	Reserved
AHB bus	0x6000 0000	EMMC bank 1 NOR/PSRAM 1/SDRAM
AHB bus	0x6400 0000	EMMC bank 1 NOR/PSRAM 2/SDRAM
AHB bus	0x6800 0000	EMMC bank 1 NOR/PSRAM 3/SDRAM
AHB bus	0x6C00 0000	EMMC bank 1 NOR/PSRAM 4/SDRAM
AHB bus	0x7000 0000	EMMC bank 2 NAND(NAND1)
AHB bus	0x8000 0000	EMMC bank 3 NAND(NAND2)
AHB bus	0x9000 0000	EMMC bank 4 PCCARD
AHB bus	0xA000 0000	EMMC Register
—	0xA000 1000	Reserved
Core	0xE000 0000	M3 Core peripheral

Note: SDRAM is directly addressed to 256M, without Bank access separately.

4.1.3. Startup configuration

At startup, the user can select one of the following three startup modes by setting the high and low levels of the Boot pin:

- Startup from main memory
- Startup from BootLoader
- Startup from built-in SRAM

The user can use USART interface to reprogram the user Flash if boot from BootLoader.

4.2. Core

The core of APM32E103VET6S is Arm® Cortex®-M3. Based on this platform, the development cost is low and the power consumption is low. It can provide excellent computing performance and advanced system interrupt response, and is compatible with all Arm tools and software.

4.3. Interrupt controller

4.3.1. Nested Vector Interrupt Controller (NVIC)

It embeds a nested vectored interrupt controller (NVIC) that can handle up to 60 maskable interrupt channels (not including 16 interrupt lines of Cortex®-M3) and 16 priority levels. The interrupt vector entry address can be directly transmitted to the core, so that the interrupt response processing with low delay can give priority to the late higher priority interrupt.

4.3.2. External Interrupt/Event Controller (EINT)

The external interrupt/event controller consists of 19 edge detectors, and each detector includes edge detection circuit and interrupt/event request generation circuit; each detector can be configured as rising edge trigger, falling edge trigger or both and can be masked independently. Up to 55 GPIOs can be connected to the 16 external interrupt lines.

4.4. On-chip memory

On-chip memory includes main memory area, SRAM and information block; the information

block includes system memory area and option byte; the system memory area stores BootLoader, 96-bit unique device ID and capacity information of main memory area; the system memory area has been written into the program and cannot be erased.

Table 5 On-chip Memory Area

Memory	Maximum capacity	Function
Main memory area	512 KB	Store user programs and data.
System memory area	2KB	Store BootLoader, 96-bit unique device ID, and main memory area capacity information
Option byte	16Bytes	Configure main memory area read-write protection and MCU working mode
SRAM	128 KB	CPU can access at 0 waiting cycle (read/write).
SDRAM	2MB	Store a large number of temporary data, it can be read to cache and data operation

Note: When using SDRAM, the operating clock of SDRAM should be 48MHz.

4.4.1. External Memory Controller（EMMC）

EMMC includes SMC (static memory controller) and DMC (dynamic memory controller). SMC is responsible for controlling SRAM, PSRAM, NandFlash, NorFlash and PC Card; DMC is responsible for controlling SDRAM.

Function:

- Three EMMC interrupt sources，through logic or connected to the NVIC list
- Write FIFO
- Code could run on external storage besides NAND Flash and PC card
- Connect with LCD

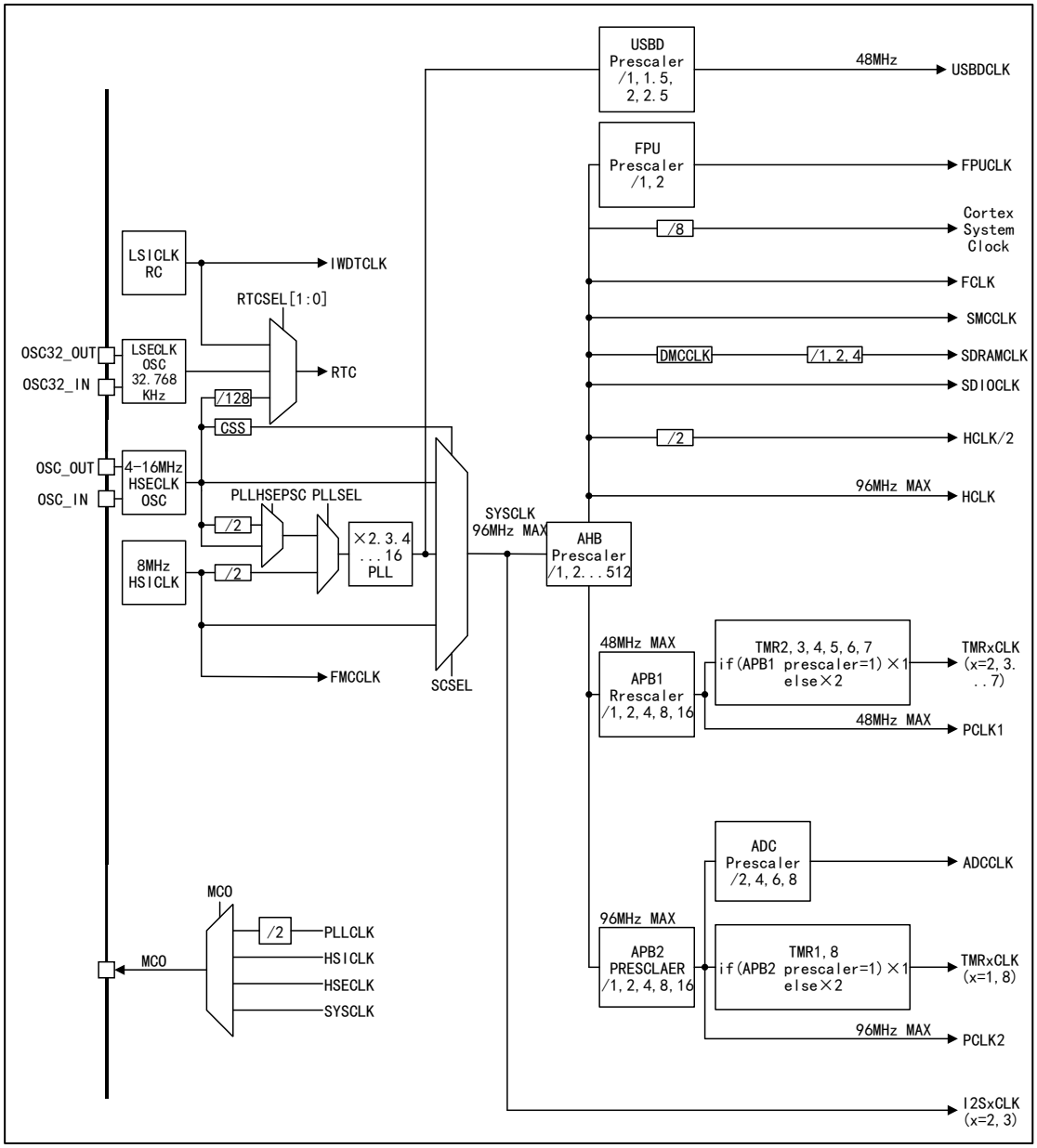
4.4.2. LCD parallel interface

EMMC can be configured to the seamless connection with most graphic LCD controller, it supports the Intel 8080 and Motorola 6800 model, and can be flexibly with specific LCD interface. Using the parallel interface LCD can be easily build simple graphics applications, or use a special scheme of high performance speed controller.

4.5. Clock

Clock tree of APM32E103VET6S is shown in the figure below:

Figure 3 APM32E103VET6S Clock Tree



4.5.1. Clock source

Clock source is divided into high-speed clock and low-speed clock according to the speed; the high-speed clock includes HSICLK and HSECLK, and the low-speed clock includes LSECLK and LSICLK; clock source is divided into internal clock and external clock according to the chip inside/outside; the internal clock includes HSICLK and LSICLK, and the external clock includes HSECLK and LSECLK, among which HSICLK is calibrated by the factory to ±1% accuracy.

4.5.2. System clock

HSICLK, PLLCLK and HSECLK can be selected as system clock; the clock source of PLLCLK can be one of HSICLK and HSECLK; the required system clock can be obtained by configuring PLL clock multiplier factor and frequency dividing coefficient.

When the product is reset and started, HSICLK is selected as the system clock by default, and

then the user can choose one of the above clock sources as the system clock by himself. When HSECLK failure is detected, the system will automatically switch to the HSICLK, and if an interrupt is enabled, the software can receive the related interrupt.

4.5.3. Bus clock

AHB, APB1 and APB2 are built in. The clock source of AHB is SYSCLK, and the clock source of APB1 and APB2 is HCLK; the required clock can be obtained by configuring the frequency dividing coefficient. The maximum frequency of AHB and high-speed APB2 is 96MHz, and the maximum frequency of APB1 is 48MHz.

4.6. Power supply and power management

4.6.1. Power supply scheme

Table 6 Power Supply Scheme

Name	Voltage range	Instruction
V_{DD}	2.0～3.6V(1)	I/Os (see pin distribution diagram for specific IO) and internal voltage regulator are powered through V_{DD} pin.
V_{DDA}/V_{SSA}	2.0～3.6V	Power supply of ADC, DAC, reset module, RC oscillator and PLL analog part; when ADC or DAC is used, V_{DDA} shall not be less than 2.4V; V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}.
V_{BAT}	1.8～3.6V	When V_{DD} is closed, RTC, external 32KHz oscillator and backup register are supplied through internal power switch.

Note : (1) Unused SDRAM, V_{DD}=2.0~3.6V; used SDRAM, V_{DD}=3.0~3.6V.

4.6.2. Voltage regulator

Table 7 Regulator Operating Mode

Name	Instruction
Master mode (MR)	Used in run mode
Low-power mode (LPR)	Used in stop mode
Power-down mode	Used in standby mode, when the voltage regulator has high impedance output, the core circuit is powered down, the power consumption of the voltage regulator is zero, and all data of registers and SRAM will be lost.

Note: The voltage regulator is always in working state after reset, and outputs with high impedance in power-down mode.

4.6.3. Power supply voltage monitor

Power-on reset (POR) and power-down reset (PDR) circuits are integrated inside the product. These two circuits are always in working condition. When the power-down reset circuit monitors that the power supply voltage is lower than the specified threshold value ($V_{POR/PDR}$), even if the external reset circuit is used, the system will remain reset.

The product has a built-in programmable voltage regulator (PVD) that can monitor V_{DD} and compare it with V_{PVD} threshold. When V_{DD} is outside the V_{PVD} threshold range and the interrupt is enabled, the MCU can be set to a safe state through the interrupt service program.

4.7. Low-power mode

APM32E103VET6S supports three low-power modes, namely, sleep mode, stop mode and standby mode, and there are differences in power, wake-up time and wake-up mode among these three modes. The low-power mode can be selected according to the actual application requirements.

Table 8 Low Power Consumption Mode

Mode	Instruction
Sleep mode	The core stops working, all peripherals are working, and it can be woken up through interrupts/events
Stop mode	Under the condition that SRAM and register data are not lost, the stop mode can achieve the lowest power consumption; The clock of the internal 1.3V power supply module will stop, HSECLK crystal resonator, HSICLK and PLL will be prohibited, and the voltage regulator can be configured in normal mode or low power mode; Any external interrupt line can wake up MCU, and the external interrupt lines include one of the 16 external interrupt lines, PVD output, RTC and USBD.
Standby mode	The power consumption in this mode is the lowest; Internal voltage regulator is turned off, all 1.3V power supply modules are powered off, HSECLK crystal resonator, HSICLK and PLL clocks are turned off, SRAM and register data disappear, RTC area and backup register contents remain, and standby circuit still works; The external reset signal on NRST, IWDT reset, rising edge on WKUP pin or RTC event will wake MCU out of standby mode.

4.8. DMA

2 built-in DMAs; DMA1 supports 7 channels and DMA2 supports 5 channels. Each channel supports multiple DMA requests, but only one DMA request is allowed to enter the DMA channel at the same time. The peripherals supporting DMA requests are ADC, SPI, USART, I2C, and TMRx. Four levels of DMA channel priority can be configured. Support "memory→memory, memory→peripheral, peripheral→memory" transfer of data (the memory includes Flash、SRAM、SDRAM)

4.9. GPIO

GPIO can be configured as general input, general output, multiplexing function and analog input、output. The general input can be configured as floating input, pull-up input and pull-down input; the general output can be configured as push-pull output and open-drain output; the multiplexing function can be used for digital peripherals; and the analog input and output can be used for analog peripherals and low-power mode; the enable and disable pull-up/pull-down resistor can be configured; the speed of 2MHz, 10MHz and 50MHz can be configured; the higher the speed is, the greater the power and the noise will be.

4.10. Communication peripherals

4.10.1. USART

Up to 3 universal synchronous/asynchronous transmitter receivers are built in the chip. The USART1 interface can communicate at a rate of 4.5Mbit/s, while other USART interfaces can communicate at a rate of 2.25Mbit/s. All USART interfaces can configure baud rate, parity check bit, stop bit, and data bit length; all USART can support DMA. USART function differences are shown in the table below:

Table 9 USART Function Differences

USART mode/function	USART1	USART2	USART3
Hardware flow control of modem	√	√	√
Synchronous mode	√	√	√
Smart card mode	√	√	√
IrDASIR coder-encoder functions	√	√	√
LIN mode	√	√	√
Single-line half-duplex mode	√	√	√
Support DMA function	√	√	√

Note: √ = support.

4.10.2. I2C

I2C1 and I2C3 bus interfaces are built in. I2C1 and I2C3 share hardware interface and register base address. Therefore, I2C1 and I2C3 cannot be used at the same time.

I2C1 can work in multiple master modes or slave modes, support 7-bit or 10-bit addressing, and support dual-slave addressing in 7-bit slave mode; the communication rate supports standard mode (up to 100kbit/s) and fast mode (up to 400kbit/s); hardware CRC generator/checker are built in; they can operate with DMA and support SMBus 2.0 version/PMBus.

I2C3 bus can operate in standard mode, fast mode and high-speed mode. The devices in high-speed mode and fast mode are downward compatible.

4.10.3. SPI/I2S

Three built-in SPIs, support full duplex and half duplex communication in master mode and slave mode, can use DMA controller, and can configure 4~16 bits per frame, and communicate at a rate of up to 18Mbit/s.

2 built-in I2S (multiplexed with SPI2 and SPI3 respectively), support half duplex communication in master mode and slave mode, support synchronous transmission, and can be configured with 16-bit, 24-bit and 32-bit data transfer with 16-bit or 32-bit resolution. The configurable range of audio sampling rate is 8kHz~48kHz; when one or two I2S interfaces are configured as the master mode, the master clock can be output to external DAC or decoder (CODEC) at 256 times of sampling frequency.

4.10.4. CAN

2 built-in CANs (CAN1 and CAN2 can be used at the same time), compatible with 2.0A and 2.0B (active) specification, and can communicate at a rate of up to 1Mbit/s. It can receive and transmit standard frame of 11-bit identifier and extended frame of 29-bit identifier. It has 3 transmit mailboxes and 2 receiving FIFOs with 3 stages, 28 adjustable filters.

4.10.5. USBD

The product embeds USBD modules (USBD1 and USBD2) compatible with full-speed USBD devices, which comply with the standard of full-speed USBD devices (12Mb/s), and the

endpoints can be configured by software, and have standby/wake-up functions. The dedicated 48MHz clock for USBD is directly generated by internal PLL. When using the USBD function, the system clock can only be one of 48MHz, 72MHz and 96MHz, which can obtain 48MHz required for USBD through 1 fractional frequency, 1.5 fractional frequency or 2 fractional frequency respectively.

USBD1 and USBD2 share register address and pin interface, so only one of them can be used at the same time.

1.1.1 Simultaneous use of USBD and CAN interfaces

This product USBD1 (2) and CAN1 (2) sharing the same dedicated 512 - byte SRAM memory used to transmit and receive data, USBD and CAN therefore be ready to use at the same time.Details are as follows:

- CAN1 and USBD2 could be used at the same time
- CAN2 and USBD1 could be used at the same time
- USBD1 and USBD2 could not be used at the same time
- CAN1 and CAN2 could be used at the same time

Note: Although there are actually 2 identical USBDs (with the same pins), they can't be used together, so it's equivalent to only 1.Users can achieve "simultaneous use" by remapping (reuse of pins).

4.11. Analog peripherals

4.11.1. ADC

3 built-in ADCs with 12-bit accuracy, up to 16 external channels and 2 internal channels for each ADC. The internal channels measure the temperature sensor voltage and reference voltage respectively. ADC1 and ADC2 have 16 external channels, ADC3 generally has 8 external channels; A/D conversion mode of each channel has single, continuous, scan or intermittent modes, ADC conversion results can be left aligned or right aligned and stored in 16 bit data register; they support analog watchdog, and DMA.

4.11.1.1. Temperature sensor

A temperature sensor (TSensor) is built in, which is internally connected with ADC_IN16 channel. The voltage generated by the sensor changes linearly with temperature, and the converted voltage value can be obtained by ADC and converted into temperature.

4.11.1.2. Internal reference voltage

Built-in reference voltage V_{REFINT}, internally connected to ADC_IN17 channel, which can be obtained through ADC; V_{REFINT} provides stable voltage output for ADC.

4.11.2. DAC

Two built-in 12-bit DACs, and each corresponding to an output channel, which can be configured in 8-bit and 12-bit modes, and the DMA function is supported. The waveform generation supports noise wave and triangle wave. The conversion mode supports independent or simultaneous conversion and the trigger mode supports external signal trigger and internal timer update trigger.

4.12. Timer

2 built-in 16-bit advanced timers (TMR1/8), 4 general-purpose timers (TMR2/3/4/5), 2 basic timers (TMR6/7), 1 independent watchdog timer, one window watchdog timer and 1 system tick timer.

Watchdog timer can be used to detect whether the program is running normally.

The system tick timer is the peripheral of the core with automatic reloading function. When the counter is 0, it can generate a maskable system interrupt, which can be used for real-time operating system and general delay.

Table 10 Function Comparison between Advanced/General-purpose/Basic and System Tick Timers

Timer type	**System tick timer**	**Basic timer**		**General-purpose timer**				**Advanced timer**	
Timer name	Sys Tick Timer	TMR6	TMR7	TMR2	TMR3	TMR4	TMR5	TMR1	TMR8
Counter resolution	24-bit	16 bits		16 bits				16 bits	
Counter type	Down	Up		Up, down, up/down				Up, down, up/down	
Prescaler coefficient	-	Any integer between 1 and 65536		Any integer between 1 and 65536				Any integer between 1 and 65536	
General DMA request	-	OK		OK				OK	
Capture/Comparison channel	-	-		4				4	
Complementary outputs	-	No		No				Yes	
Pin characteristics	-	-		There are 5 pins in total: 1-way external trigger signal input pins, 4-way channel (non-complementary channel) pins				There are 9 pins in total: 1-way external trigger signal input pins, 1-way braking input signal pins, 3-pair complementary channel pins, 1-way channel (non-complementary channel) pins	
Function Instruction	Special for real-time operating system Automatic reloading function supported When the counter is 0, it can generate a maskable system interrupt Can program the clock source	Used to generate DAC trigger signals. Can be used as a 16-bit general-purpose timebase counter.		Synchronization or event chaining function provided Timers in debug mode can be frozen. -Can be used to generate PWM output Each timer has independent DMA request generation. It can handle incremental encoder signals				It has complementary PWM output with dead band insertion When configured as a 16-bit standard timer, it has the same function as the TMRx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0~100%).	

Timer type	System tick timer	Basic timer	General-purpose timer	Advanced timer
				In debug mode, the timer can be frozen, and PWM output is disabled. Synchronization or event chaining function provided.

Table 11 Independent Watchdog and Window Watchdog Timers

Name	Counter resolution	Counter type	Prescaler coefficient	Functional Description
Independent watchdog	12-bit	Down	Any integer between 1 and 256	The clock is provided by an internally independent RC oscillator, which is independent of the master clock, so it can run in stop and standby modes. The whole system can be reset in case of problems. It can provide timeout management for applications as a free-running timer. It can be configured as a software or hardware startup watchdog through option bytes. Timers in debug mode can be frozen.
Window watchdog	7-bit	Down	-	Can be set for free running. The whole system can be reset in case of problems. Driven by the master clock, it has early interrupt warning function; Timers in debug mode can be frozen.

4.13. RTC

1 RTC is built in, and there are LSECLK signal input pins (OSC32_IN and OSC32_OUT) and 1 TAMP input signal detection pin (TAMP); the clock source can select external 32.768kHz crystal oscillator, resonator or oscillator, LSICLK and HSECLK/128; it is supplied by V_{DD} by default; when V_{DD} is powered off, it can be automatically switched to V_{BAT} power supply, and RTC configuration and time data will not be lost; RTC configuration and time data are not lost in case of system resetting, software resetting and power resetting; it supports clock and calendar functions.

4.13.1. Backup register

84-byte backup register is built in, and is supplied by V_{DD} by default; when V_{DD} is powered off, it can be automatically switched to V_{BAT} power supply, and the data in backup register will not be lost; the data in backup register will not be lost in case of system resetting, software resetting and power resetting.

4.14. CRC

A CRC (cyclic redundancy check) calculation unit is built in, which can generate CRC codes and operate 8-bit, 16-bit and 32-bit data.

4.15. FPU

The product has built-in independent FPU floating-point operation processing unit, supports IEEE754 standard, supports single-precision floating-point operation, and supports algorithms such as CMP, SUM, SUB, PRDCT, MAC, DIV, INVRGSQT, RGSQT, SUMSQ, DOT, floating-point to integer conversion and integer to floating point conversion.

5. Electrical characteristics

5.1. Test conditions of electrical characteristics

5.1.1. Maximum and minimum values

Unless otherwise specified, all products are tested on the production line at TA=25℃. Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data are obtained through comprehensive evaluation, design simulation or process characteristics and are not tested on the production line; on the basis of comprehensive evaluation, after passing the sample test, take the average value and add and subtract three times the standard deviation (average ±3∑) to get the maximum and minimum values.

5.1.2. Typical value

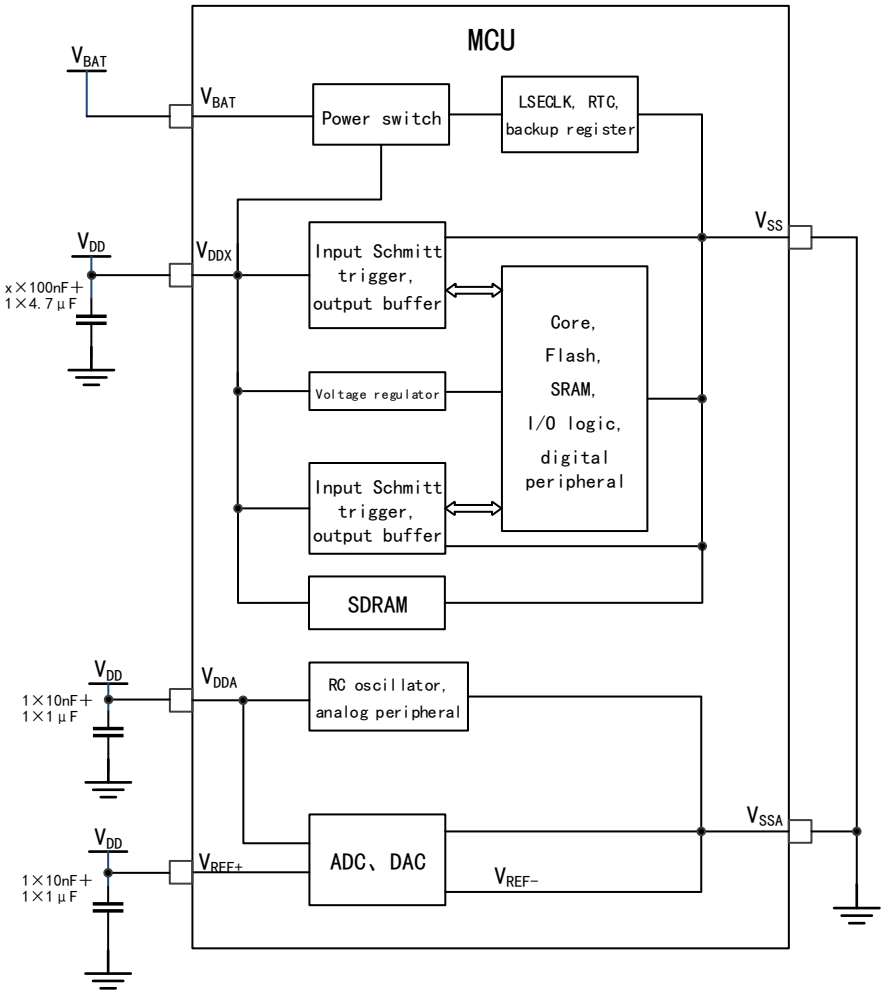
Unless otherwise specified, typical data are measured based on TA=25℃, V_{DD}=V_{DDA}=3.3V. these data are only used for design guidance.

5.1.3. Typical curve

Unless otherwise specified, typical curves will only be used for design guidance and will not be tested.

5.1.4. Power supply scheme

Figure 4 Power Supply Scheme



Notes: V_{DD}x in the figure means the number of V_{DD} is x

5.1.5. Load capacitance

Figure 5 Load conditions when measuring pin parameters

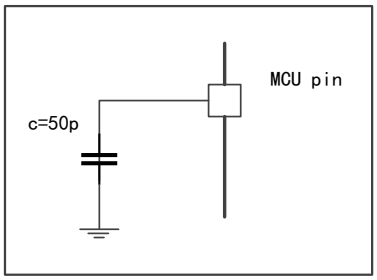


Figure 6 Pin Input Voltage Measurement Scheme

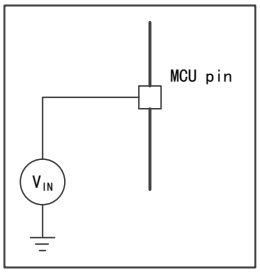
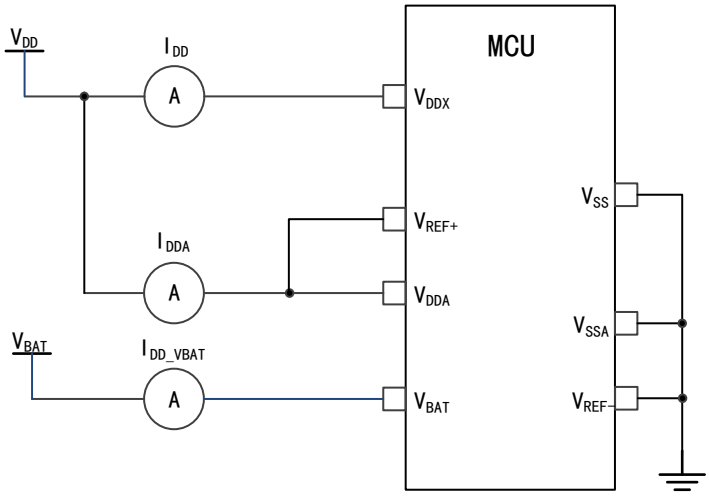


Figure 7 Power Consumption Measurement Scheme



5.2. Test under general operating conditions

Table 12 General Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	96	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	-	48	
f_{PCLK2}	Internal APB2 clock frequency	-	-	96	
V_{DD}	Main power supply voltage（Unused SDRAM）	-	2	3.6	V
	Main power supply voltage（Used SDRAM）	-	3	3.6	
V_{DDA}	Analog power supply voltage (When neither ADC nor DAC is used)	Must be the same as V_{DD}	V_{DD}	3.6	V
	Analog power supply voltage (When ADC and DAC are used)		2.4	3.6	
V_{BAT}	Power supply voltage of backup domain	-	1.8	3.6	V
T_A	Ambient temperature (temperature number 6)	Maximum power dissipation	-40	85	℃

Note: During power-up and normal operation, it is recommended to use the same power supply for V_{DD} and V_{DDA}, with a maximum voltage difference of 300 mV between V_{DD} and V_{DDA}.

5.3. Absolute maximum ratings

If the load on the device exceeds the absolute maximum rating, it may cause permanent damage to the device. Here, only the maximum load that can be borne is given, and there is no guarantee that the device functions normally under this condition.

5.3.1. Maximum temperature characteristics

Table 13 Temperature Characteristics

Symbol	Description	Numerical Value	Unit
T_{STG}	Storage temperature range	-55 ~ +150	℃
T_J	Maximum junction temperature	105	℃

5.3.2. Maximum rated voltage characteristics

All power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the power supply within the external limited range.

Table 14 Maximum Rated Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
V_{DD} - V_{SS}	External main power supply voltage	-0.3	4.0	V
V_{DDA}-V_{SSA}	External analog power supply voltage	-0.3	4.0	
V_{BAT}-V_{SS}	Power supply voltage of external backup domain	-0.3	4.0	
| V_{DD}-V_{DDA} |	Voltage difference allowed by V_{DD}>V_{DDA}	-	0.3	
V_{IN}	Input voltage on FT pins	V_{SS}-0.3	5.5	
	Input voltage on other pins	V_{SS}-0.3	V_{DD} + 0.3	
| ΔV_{DDx} |	Voltage difference between different power supply pins	-	50	mV
| V_{SSx}-V_{SS} |	Voltage difference between different grounding pins	-	50	

5.3.3. Maximum rated current features

Table 15 Current Characteristics

Symbol	Description	Maximum	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Irrigation current on any I/O and control pins	25	
	Source current on any I/O and control pins	-25	
$I_{INJ(PIN)}$ (2)	Injection current of 5T pin(3)	-5/+0	
	Injection current of other pins(4)	±5	
$\Sigma I_{INJ(PIN)}$(2)	Total injection current on all I/O and control pins (5)	±25	

（1） All power (V_{DD}，V_{DDA}) and ground (V_{SS}，V_{SSA}) pins must always be connected to a power supply within the external allowable range.

（2） Negative injection disturbs the analog performance of the device.

（3） Positive injection is not possible on these I/Os. a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded.

（4） A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded.

（5） When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

5.3.4. Electrostatic discharge (ESD)

Table 16 ESD Absolute Maximum Ratings

Symbol	Parameter	Conditions	Value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25℃	±5000	V

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.3.5. Static latch-up (LU)

Table 17 Static Latch-up

Symbol	Parameter	Conditions	Type
LU	Class of static latch-up	T_A = +25℃/85℃, conforming to EIA/JESD78E	CLASS Ⅱ A

Note: The samples are measured by a third-party testing organization and are not tested in production.

5.4. On-chip memory

5.4.1. Flash characteristics

Table 18 Flash Memory Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
tprog	16-bit programming time	T_A = -40~85℃ V_{DD}=2.4~3.6V	40	46.08	70	μs
t_{ERASE}	Page (2KBytes) erase time	T_A = -40~85℃ V_{DD}=2.4~3.6V	10	-	30	ms
t_{ME}	Whole erase time	T_A = -40~85℃ V_{DD}=2.4~3.3V	10	-	30	ms
Vprog	Programming voltage	T_A = -40~85℃	2	-	3.6	V
t_{RET}	Data saving time	T_A=125℃	10.77	-	-	years
N_{RW}	Erase cycle	T_A=85°C	100K	-	-	cycles

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5. Clock

5.5.1. Characteristics of external clock source

5.5.1.1. High-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 19 HSECLK4~16MHz Oscillator Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
RF	Feedback resistance	-	-	200	-	kΩ
$I_{DD(HSECLK)}$	HSECLK current consumption	V_{DD}=3.3V, CL=10pF@8MHz	-	-	0.56	mA
$t_{SU(HSECLK)}$	Startup time	V_{DD} is stable	-	0.85	-	ms

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5.1.2. Low-speed external clock generated by crystal resonator

For detailed parameters (frequency, package, precision, etc.) of crystal resonator, please consult the corresponding manufacturer.

Table 20 LSECLK Oscillator Characteristics (f_{LSECLK}=32.768KHz)

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f_{OSF_IN}	Oscillator frequency	-	-	32.768	-	KHz
$I_{DD(LSECLK)}$	LSECLK current consumption	-	-	-	0.8	μA
$t_{SU(LSECLK)}$(1)	Startup time	V_{DDIOx} is stable	-	0.93	-	s

Note: It is obtained from a comprehensive evaluation and is not tested in production.

（1） $t_{SU(LSECLK)}$ is the startup time, which is measured from the time when LSECLK is enabled by software to the time when stable oscillation at 32.768KHz is obtained. This value is measured using a standard crystal resonator, which may vary greatly due to different crystal manufacturers.

5.5.2. Characteristics of internal clock source

5.5.2.1. High speed internal (HSICLK) RC oscillator

Table 21 HSICLK Oscillator Characteristics

Symbol	Parameter	Conditions		Minimum value	Typical value	Maximum value	Unit
f_{HSICLK}	Frequency	-		-	8	-	MHz
$A_{CCHSICLK}$	Accuracy of HSICLK oscillator	Factory calibration	V_{DD}=3.3V, T_A=25℃(1)	-1	-	1	%
			V_{DD}=2-3.6V, T_A=-40~85℃	-1.5	-	1.5	%

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$I_{DDA(HSICLK)}$	Power consumption of HSICLK oscillator	-	-	-	76	μA
$t_{SU(HSICLK)}$	Startup time of HSICLK oscillator	V_{DD}=3.3V，T_A=-40~85℃	3.24	-	3.4	μs

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5.2.2. Low speed internal (LSICLK) RC oscillator

Table 22 LSICLK Oscillator Characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
f_{LSICLK}	Frequency (V_{DD} =2-3.6V, T_A =-40~85℃)	30	40	60	KHz
$I_{DD(LSICLK)}$	Power consumption of LSICLK oscillator	-	-	0.56	μA
$t_{SU(LSICLK)}$	LSICLK oscillator startup time, (V_{DD}=3.3V, T_A=-40~85℃)	-	-	74.8	μs

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.5.3. PLL Characteristics

Table 23 PLL Characteristics

Symbol	Parameter	Numerical Value			Unit
		Minimum value	Typical value	Maximum value	
f_{PLL_IN}	PLL input clock	1	8	25	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL frequency doubling output clock, (V_{DD}=3.3V, T_A=-40~85℃)	16	-	96	MHz
t_{LOCK}	PLL phase locking time	-	-	200	μs

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.6. Reset and power management

5.6.1. Power-on/power-down characteristics

Table 24 Power-on/power-down Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{VDD}	V_{DD} rise time rate	-	1	-	200000	μs/V
	V_{DD} fall time rate		1	-	200000	

5.6.2. Test of embedded reset and power control block characteristics

Table 25 Embedded Reset and Power Control Block Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.84	1.86	1.88	V
		Rising edge	1.90	1.92	1.93	V
$V_{PDRhyst}$	PDR hysteresis	-	50.00	54.00	60.00	mV
$T_{RSTTEMPO}$	Reset duration	-	0.90	1.39	4.90	ms

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table 26 Programmable Power Supply Voltage Detector Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{PVD}	Programmable power supply voltage detector voltage level selection	PLS[2:0]=000 (rising edge)	2.17	-	2.20	V
		PLS[2:0]=000 (falling edge)	2.06	-	2.10	V
		PLS[2:0]=000(PVD hysteresis)	100	-	110	mV
		PLS[2:0]=001 (rising edgeg)	2.27	-	2.30	V
		PLS[2:0]=001 (falling edge)	2.16	-	2.19	V
		PLS[2:0]=001(PVD hysteresis)	110	-	120	mV
		PLS[2:0]=010 (rising edgeg)	2.37	-	2.40	V
		PLS[2:0]=010 (falling edge)	2.26	-	2.29	V
		PLS[2:0]=010(PVD hysteresis)	100	-	110	mV
		PLS[2:0]=011 (rising edgeg)	2.46	-	2.50	V
		PLS[2:0]=011 (falling edge)	2.36	-	2.39	V
		PLS[2:0]=011(PVD hysteresis)	100	-	110	mV
		PLS[2:0]=100 (rising edgeg)	2.57	-	2.60	V
		PLS[2:0]=100 (falling edge)	2.45	-	2.49	V
		PLS[2:0]=100(PVD hysteresis)	110	-	120	mV
		PLS[2:0]=101 (rising edgeg)	2.66	-	2.70	V
		PLS[2:0]=101 (falling edge)	2.56	-	2.59	V
		PLS[2:0]=101(PVD hysteresis)	100	-	110	mV
		PLS[2:0]=110 (rising edgeg)	2.76	-	2.80	V
		PLS[2:0]=110 (falling edge)	2.65	-	2.69	V
		PLS[2:0]=110(PVD hysteresis)	110	-	110	mV
		PLS[2:0]=111 (rising edgeg)	2.87	-	2.91	V
		PLS[2:0]=111 (falling edge)	2.75	-	2.79	V

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
		PLS[2:0]=111(PVD hysteresis)	110	-	120	mV

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.7. Power consumption

5.7.1. Power consumption test environment

（1） The values are measured by executing Dhrystone 2.1, with the Keil.V5 compilation environment and the L0 compilation optimization level.

（2） All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)

（3） Unless otherwise specified, all peripherals are turned off

（4） The relationship between Flash waiting cycle setting and f_{HCLK} :

0~24MHz: 0 waiting cycle

24~48MHz: 1 waiting cycle

48~72MHz: 2 waiting cycles

72~96MHz: 3 waiting cycles

The instruction prefetch function is enabled (Note: it must be set before clock setting and bus frequency division)

（5） When the peripherals are enabled: $f_{PCLK1}=f_{HCLK}/2$，$f_{PCLK2}=f_{HCLK}$

5.7.2. Power consumption in run mode

Table 27 Power Consumption in Run Mode when the Program is Executed in Flash while SDRAM is in run mode

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=85℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
Power consumption in run mode	HSECLK bypass (2) , enabling all peripherals	96MHz	226.47	30.08	242.85	36.79
		72MHz	176.23	23.83	190.75	30.08
		48MHz	128.30	16.97	141.19	22.31
		36MHz	105.04	13.87	117.18	18.89
		24MHz	128.37	10.10	140.78	14.55
		16MHz	97.44	7.43	109.48	11.70
		8MHz	18.48	4.72	30.64	8.64
	HSECLK bypass (2) , turning off all peripherals	96MHz	226.24	21.79	241.33	28.21
		72MHz	176.20	17.87	188.46	23.92
		48MHz	128.30	12.81	137.84	17.75
		36MHz	104.94	10.62	114.74	15.44
		24MHz	128.29	8.07	138.24	12.45
		16MHz	97.38	6.14	107.58	10.31
		8MHz	18.47	4.05	29.07	7.83
	HSICLK (2) , enabling all peripherals	64MHz	244.37	21.24	263.71	27.05
		48MHz	212.97	16.54	230.53	21.98
		36MHz	190.00	13.32	206.42	18.30
		24MHz	167.25	9.67	183.49	14.27
		16MHz	182.26	7.11	198.32	11.20
		8MHz	103.97	4.40	119.01	8.01
	HSICLK (2) , turning off all peripherals	64MHz	244.38	16.12	263.41	21.78
		48MHz	212.89	12.44	230.32	17.16
		36MHz	189.92	10.34	206.30	15.06
		24MHz	167.20	7.80	183.63	12.18
		16MHz	182.21	5.86	198.52	9.95
		8MHz	103.93	3.75	117.60	7.51

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

Table 28 Power Consumption in Run Mode when the Program is Executed in RAM while SDRAM is in run mode

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=85℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
Power consumption in run mode	HSECLK bypass (2) , enabling all peripherals	96MHz	226.32	22.57	242.85	36.79
		72MHz	176.21	17.11	190.75	30.08
		48MHz	128.46	12.07	141.19	22.31
		36MHz	104.97	9.64	117.18	18.89
		24MHz	128.41	6.82	140.78	14.55
		16MHz	97.41	5.04	109.48	11.70
		8MHz	18.48	3.24	30.64	8.64
	HSECLK bypass (2) , turning off all peripherals	96MHz	226.38	12.60	241.33	28.21
		72MHz	176.15	9.83	188.46	23.92
		48MHz	128.33	6.95	137.84	17.75
		36MHz	104.99	5.44	114.74	15.44
		24MHz	128.36	4.10	138.24	12.45
		16MHz	97.41	3.18	107.58	10.31
		8MHz	18.46	2.21	29.07	7.83
	HSICLK (2) , enabling all peripherals	64MHz	244.38	15.17	263.71	27.05
		48MHz	212.97	11.59	230.53	21.98
		36MHz	189.91	9.04	206.42	18.30
		24MHz	167.25	6.18	183.49	14.27
		16MHz	182.26	4.46	198.32	11.20
		8MHz	103.88	2.69	119.01	8.01
	HSICLK (2) , turning off all peripherals	64MHz	244.33	8.65	263.41	21.78
		48MHz	212.87	6.69	230.32	17.16
		36MHz	189.92	5.13	206.30	15.06
		24MHz	167.25	3.78	183.63	12.18
		16MHz	182.25	2.86	198.52	9.95
		8MHz	103.91	1.88	117.60	7.51

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL.

5.7.3. Power consumption in sleep mode

Table 29 Power Consumption in Sleep Mode when the Program is Executed in Flash while SDRAM is in run mode

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=85℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
Power consumption in sleep mode	HSECLK bypass (2) , enabling all peripherals	96 MHz	226.36	22.76	241.84	29.02
		72MHz	176.09	17.72	188.95	23.81
		48MHz	128.36	12.56	137.94	17.67
		36MHz	104.95	10.03	113.29	14.31
		24MHz	128.30	7.26	137.94	11.38
		16MHz	97.42	5.43	106.53	9.47
		8MHz	18.47	3.61	28.11	7.37
	HSECLK bypass (2) , turning off all peripherals	96 MHz	226.19	13.92	241.69	20.08
		72MHz	176.06	11.01	188.63	16.92
		48MHz	128.23	7.90	137.86	13.08
		36MHz	104.86	6.39	113.63	11.17
		24MHz	128.15	4.92	137.74	9.27
		16MHz	97.30	3.90	106.08	7.89
		8MHz	18.45	2.80	27.91	6.53
	HSICLK (2) , enabling all peripherals	64MHz	244.26	15.80	263.45	22.17
		48MHz	212.87	12.37	230.41	18.58
		36MHz	189.91	9.72	206.26	15.30
		24MHz	167.19	6.88	183.49	12.52
		16MHz	182.22	5.14	198.33	9.09
		8MHz	103.92	3.29	116.64	6.96
	HSICLK (2) , turning off all peripherals	64MHz	244.21	9.70	263.33	15.06
		48MHz	212.78	7.55	230.15	12.70
		36MHz	189.78	6.12	205.73	10.74
		24MHz	167.14	4.59	182.01	8.86
		16MHz	182.15	3.56	197.25	7.54
		8MHz	103.90	2.49	116.82	6.49

Table 30 Power Consumption in Sleep Mode when the Program is Executed in RAM while SDRAM is in run mode

Parameter	Conditions	f_{HCLK}	Typical value (1)		Maximum value (1)	
			T_A=25℃，V_{DD}=3.3V		T_A=85℃，V_{DD}=3.6V	
			I_{DDA}(μA)	I_{DD}(mA)	I_{DDA}(μA)	I_{DD}(mA)
Power consumption in sleep mode	HSECLK bypass (2) , enabling all peripherals	96MHz	226.45	14.97	241.17	18.07
		72MHz	176.19	11.68	188.22	14.90
		48MHz	128.30	8.38	137.29	11.74
		36MHz	104.88	6.67	112.85	10.07
		24MHz	128.41	4.72	137.58	8.07
		16MHz	97.46	3.58	105.18	6.99
		8MHz	18.46	2.40	23.22	5.80
	HSECLK bypass (2) , turning off all peripherals	96MHz	226.02	3.91	241.07	7.31
		72MHz	175.91	3.25	187.99	6.65
		48MHz	128.08	2.58	137.41	5.98
		36MHz	104.87	2.22	112.77	5.62
		24MHz	128.19	1.92	137.35	5.33
		16MHz	97.31	1.72	105.00	5.12
		8MHz	18.45	1.44	22.08	4.84
	HSICLK (2) , enabling all peripherals	64MHz	244.38	10.24	262.32	13.48
		48MHz	212.87	7.95	229.35	11.39
		36MHz	189.83	6.33	205.46	9.72
		24MHz	166.95	4.38	182.91	7.72
		16MHz	182.12	3.27	197.75	6.62
		8MHz	103.78	2.08	117.28	5.46
	HSICLK (2) , turning off all peripherals	64MHz	244.11	2.72	262.65	6.10
		48MHz	212.70	2.27	229.17	5.66
		36MHz	189.73	1.90	205.26	5.30
		24MHz	167.11	1.59	182.02	4.98
		16MHz	182.10	1.39	197.38	4.78
		8MHz	103.83	1.12	117.18	4.51

Note:

(1) It is obtained from a comprehensive evaluation and is not tested in production.

(2) The external clock is 8MHz, and when f_{HCLK}>8MHz, turn on PLL, otherwise, turn off PLL

5.7.4. Power consumption in stop mode and standby mode

Table 31 Power Consumption in Stop Mode and Standby Mode

Parameter	Conditions	Typical value (1), (T_A=25℃)						Maximum value (1), (V_{DD}=3.6V)	
		V_{DD}=3.3V		V_{DD}=3.3V		V_{DD}=3.6V		T_A=85℃	
		I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)	I_{DDA} (μA)	I_{DD} (μA)
Power consumption in stop mode	Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog)	4.04	255.55	4.31	256.61	4.68	257.65	5.85	563.30
	Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog)	4.05	250.24	4.30	251.23	4.67	253.14	5.81	529.20
Power consumption in standby mode	Low-speed internal RC oscillator and independent watchdog ON	3.42	205.16	3.77	205.67	4.27	206.25	5.03	216.64
	Low-speed internal RC oscillator on, independent watchdog OFF	3.42	205.11	3.77	205.51	4.26	206.11	5.03	216.32
	Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	2.70	204.79	2.96	205.25	3.34	205.80	4.23	216.19

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

5.7.5. Backup domain power consumption

Table 32 Backup Domain Power Consumption

Symbol	Conditions	Typical value (1), T_A=25℃			Maximum value (1), V_{BAT}=3.6V		Unit
		V_{BAT}=1.8V	V_{BAT}=2.4V	V_{BAT}=3.3V	T_A=25℃	T_A=85℃	
$I_{DD}\_V_{BAT}$	The low-speed oscillator and RTC are in ON state	1.106	1.268	1.704	1.956	2.568	μA

Note: (1) It is obtained from a comprehensive evaluation and is not tested in production.

5.8. Wake-up time in low power mode

The measurement of wake-up time in low power mode is from the start of wake-up event to the time when the user program reads the first instruction, in which V_{DD}=V_{DDA}.

Table 33 Wake Up Time in Low-power Mode

Symbol	Parameter	Conditions	Min	Typical value (T_A=25℃)			Max	Unit
				2V	3.3V	3.6V		
$t_{WUSLEEP}$	Wake-up from sleep mode	-	0.52	0.61	0.60	0.57	0.65	μs
t_{WUSTOP}	Wake up from stop mode	The voltage regulator is in run mode	1.83	2.24	1.91	1.86	2.26	
		The voltage regulator is in low power mode	2.66	4.18	2.95	2.82	4.61	
$t_{WUSTDBY}$	Wake up from standby mode	-	59.56	76.40	63.74	61.29	84.56	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.9. Pin characteristics

5.9.1. I/O pin characteristics

Table 34 DC Characteristics (test condition of V_{DD}=2.7~3.6V, T_A=-40~85℃)

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{IL}	Low level input voltage	CMOS port	-0.5	-	0.35V_{DD}	V
V_{IH}	High level input voltage		0.65V_{DD}	-	V_{DD}+0.5	
V_{IL}	Low level input voltage	TTL port	-0.5	-	0.8	
V_{IH}	High level input voltage, Standard I/O port		2	-	V_{DD}+0.5	
	High level input voltage, I/O FT port		2		5.5	
V_{hys}	Standard I/O Schmitt trigger voltage hysteresis	-	200	-	-	mV
	I/O FT Schmitt trigger voltage hysteresis		5%V_{DD}	-	-	mV
I_{lkg}	Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/O port	-	-	±1	μA
		V_{IN}=5V, I/O FT port	-	-	3	
R_{PU}	Weak pull-up equivalent resistance	$V_{IN}=V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistance	$V_{IN}=V_{DD}$	30	40	50	kΩ

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table 35 AC Characteristics

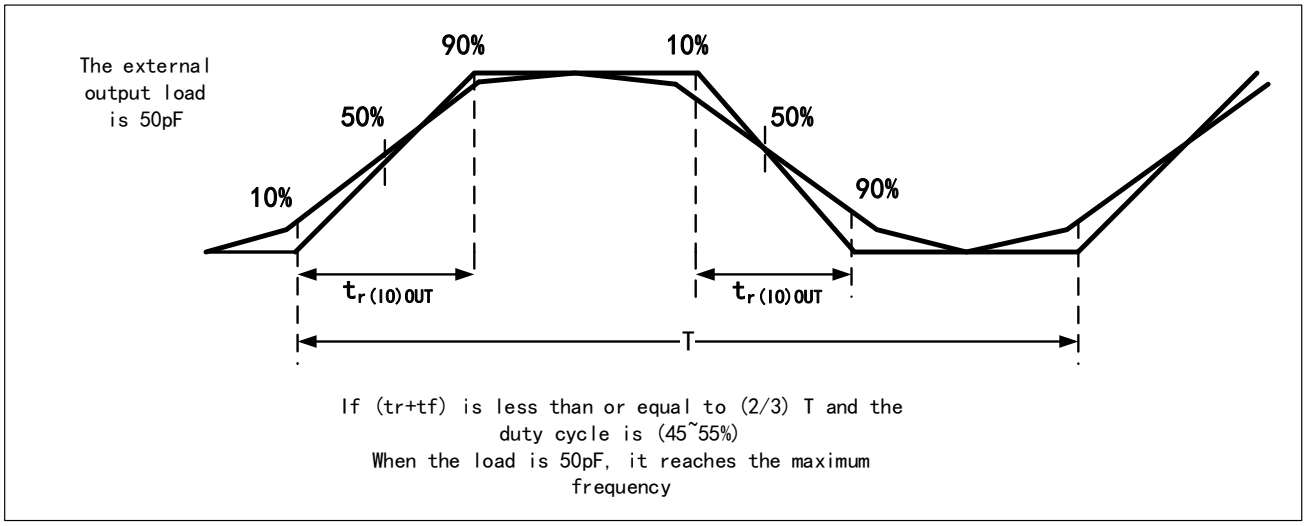
MODEy[1:0] Configuration	Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
10 (2MHz)	fmax(IO)out	Maximum frequency	CL=50 pF, V_{DD}=2~3.6V	-	2	MHz
	tf(IO)out	Output fall time from high to low level	CL=50 pF, V_{DD} =2~3.6V	-	125	ns
	tr(IO)out	Output rise time from low to high level		-	125	
01 (10MHz)	fmax(IO)out	Maximum frequency	CL=50 pF, V_{DD} =2~3.6V	-	10	MHz
	tf(IO)out	Output fall time from high to low level	CL=50 pF,	-	25	ns

MODEy[1:0] Configuration	Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
	tr(IO)out	Output rise time from low to high level	V_{DD} =2~3.6V	-	25	
11 (50MHz)	fmax(IO)out	Maximum frequency	CL=30 pF, V_{DD} =2.7~3.6V	-	50	MHz
	tf(IO)out	Output fall time from high to low level	CL=30 pF, V_{DD} =2.7~3.6V	-	5	ns
	tr(IO)out	Output rise time from low to high level		-	5	

Note: (1) The rate of I/O port can be configured through MODEy.

(2) The data are obtained from a comprehensive evaluation and is not tested in production.

Figure 8 I/O AC Characteristics Definition



Note: It is obtained from a comprehensive evaluation and is not tested in production.

Table36 Output Drive Current Characteristics (test condition V_{DD}=2.7~3.6V, T_A=-40~85℃)

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
V_{OL}	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +8mA 2.7V<V_{DD}<3.6V	-	0.49	V
V_{OH}	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}-0.4	-	
V_{OL}	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20mA 2.7V<V_{DD}<3.6V	-	1.50	V
V_{OH}	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}-1.2	-	

5.9.2. NRST pin characteristics

The NRST pin input drive adopts CMOS process, which is connected with a permanent pull-up resistor R_{PU}.

Table 37 NRST Pin Characteristics (test condition V_{DD}=3.3V, T_A=-40~85℃)

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$V_{IL(NRST)}$	NRST low level input voltage	-	-0.5	-	0.8	V
$V_{IH(NRST)}$	NRST high level input voltage	-	2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
RPU	Weak pull-up equivalent resistance	$V_{IN} = V_{SS}$	30	40	50	kΩ

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.10. Communication peripherals

5.10.1. I2C peripheral characteristics

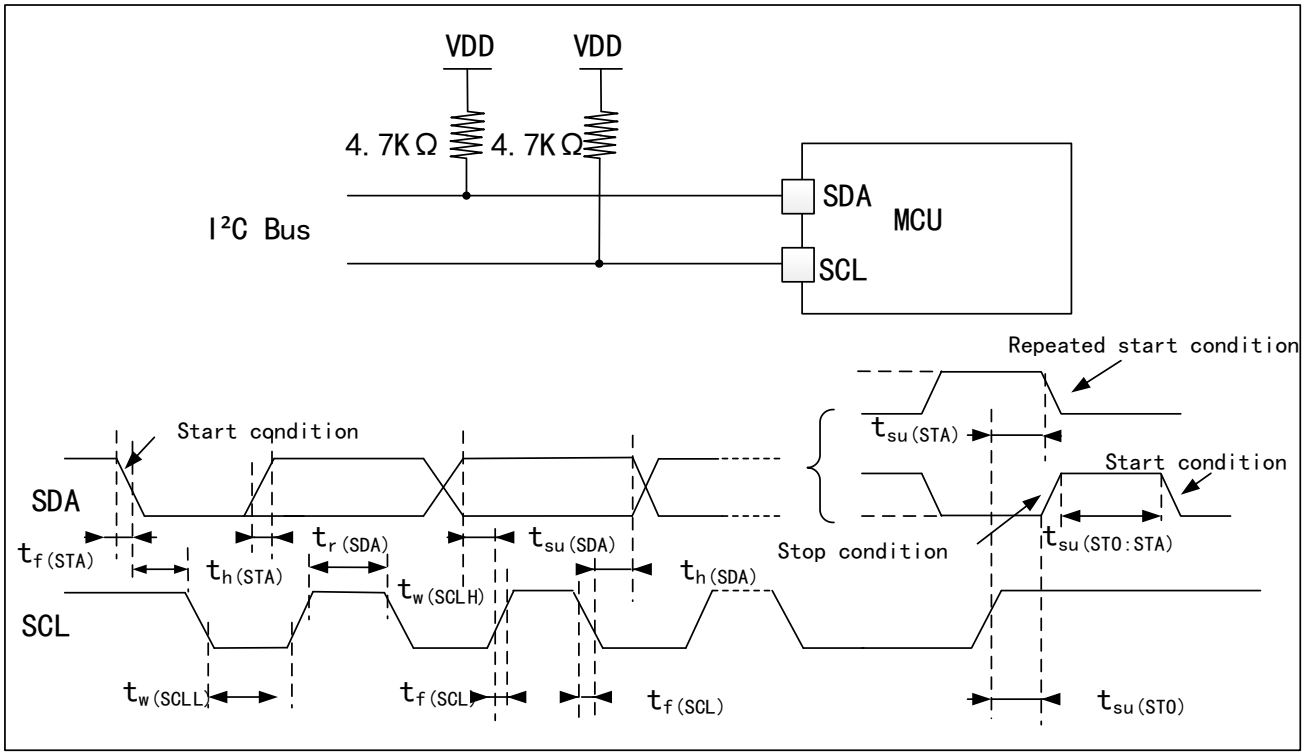
To achieve maximum frequency of I2C in standard mode, f_{PCLK1} must be greater than 2MHz. To achieve maximum frequency of I2C in fast mode, f_{PCLK1} must be greater than 4MHz.

Table 38 I2C Interface Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	-	3450	-	900	
$t_{r(SDA)}/t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}/t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	μs
$t_{su(STA)}$	Repeated start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Setup time of stop condition	4.0	-	0.6	-	
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	4.7	-	1.3	-	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Figure 9 I2C Bus AC Waveform and Measurement Circuit



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.10.2. SPI peripheral characteristics

Table 39 SPI Characteristics (T_A=25℃, V_{DD}=3.3V)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SI clock rise and fall time	Load capacitance: C = 30pF	-	8	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{PCLK}$	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Main mode, f_{PCLK} = 36MHz, Prescaler coefficient=4	50	60	ns
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	5	-	ns
		Slave mode	5	-	
$t_{h(MI)}$ $t_{h(SI)}$	Data input hold time	Master mode	5	-	ns
		Slave mode	4	-	
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK} = 20MHz	0	$3t_{PCLK}$	ns
$t_{dis(SO)}$	Data output prohibition time	Slave mode	2	10	ns
$t_{v(SO)}$	Effective time of data output	Slave mode (after enable edge)	-	25	ns

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(MO)}$	Effective time of data output	Master mode (after enable edge)	-	5	ns
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	15	-	ns
$t_{h(MO)}$		Master mode (after enable edge)	2	-	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

Figure 10 SPI Timing Diagram - Slave Mode and CPHA=0

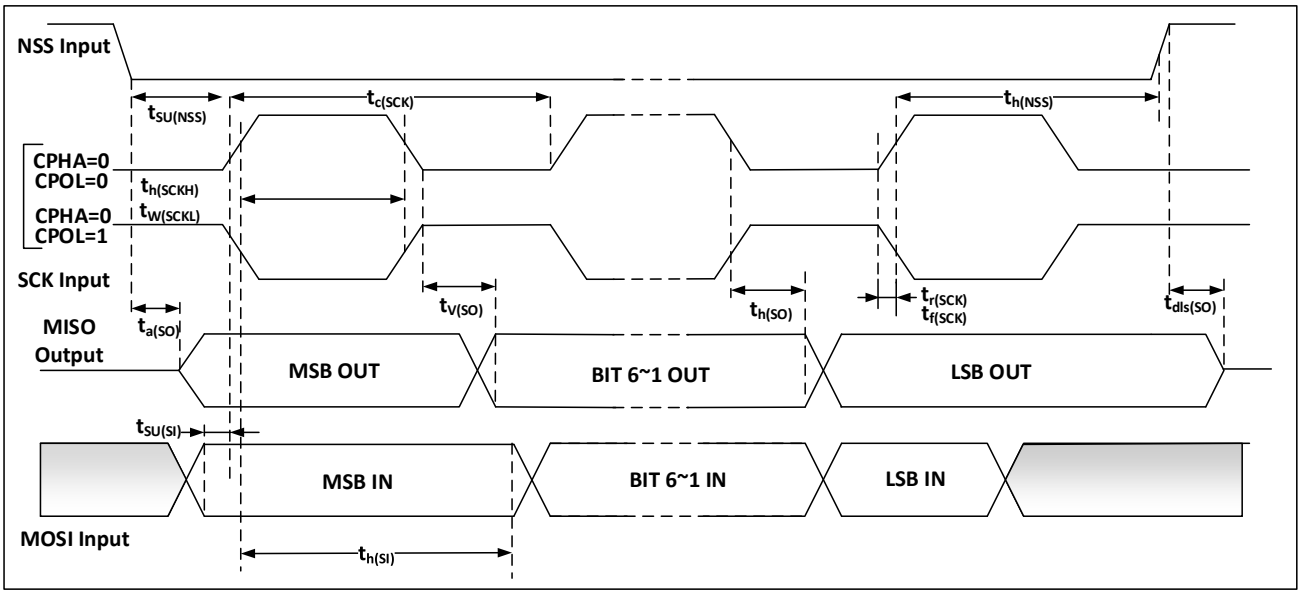
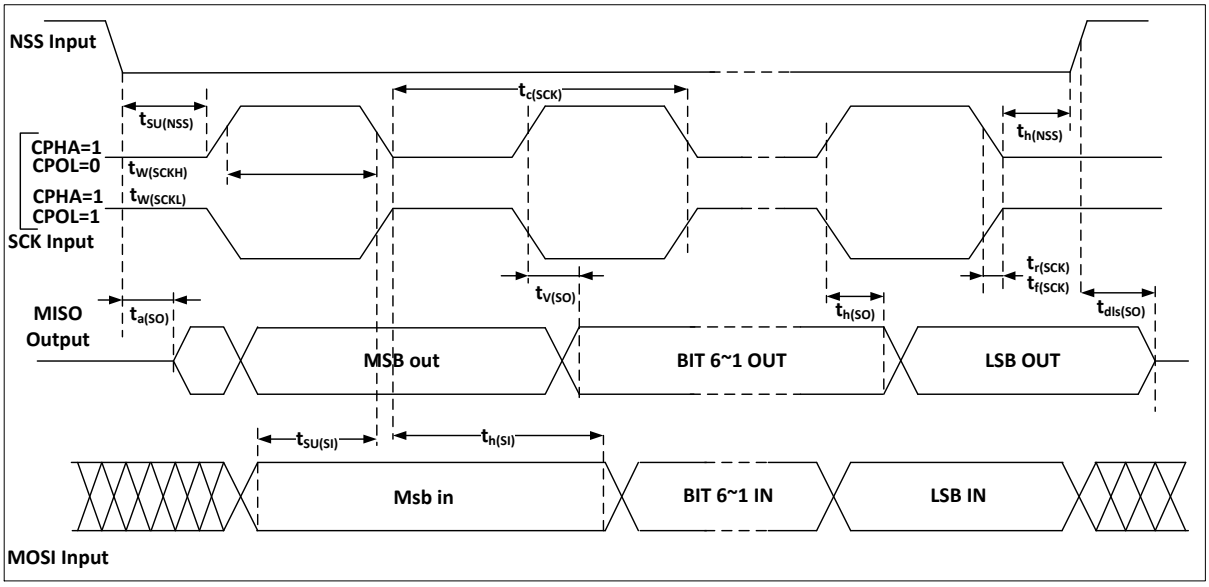
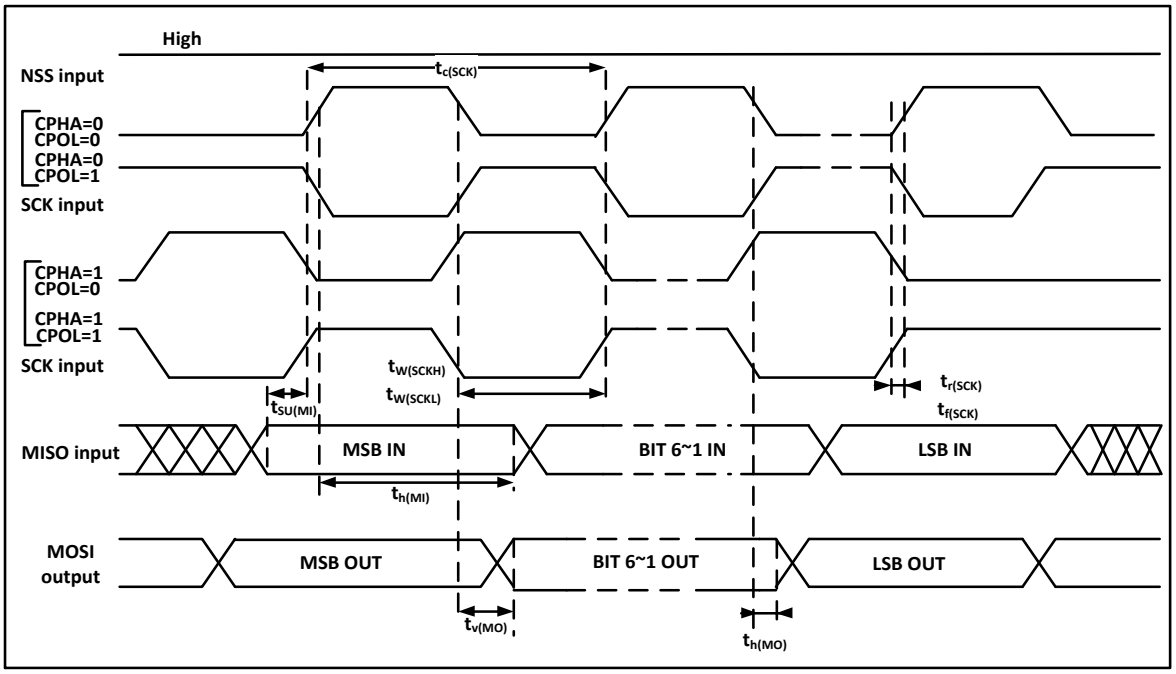


Figure 11 SPI Timing Diagram - Slave Mode and CPHA=1



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 12 SPI Timing Diagram - Master Mode



Note: The measuring points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.11. Analog peripherals

5.11.1. ADC

Test parameter description:

- Sampling rate: the number of conversion of analog quantity to digital quantity by ADC per second
  Sample rate=ADC clock/(number of sampling periods + number of conversion periods)

5.11.1.1. 12-bit ADC characteristics

Table 40 12-bit ADC Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{DDA}	Power supply voltage	-	2.4	-	3.6	V
I_{DDA}	ADC pwoer consumption	V_{DDA}=3.3V，f_{ADC}=14MHz，Sampling time=1.5 f_{ADC}	-	1	-	mA
f_{ADC}	ADC frequency	-	0.6	-	14	MHz
C_{ADC}	Internal sampling and holding capacitance	-	-	8	-	pF
R_{ADC}	Sampling resistor	-	-	-	1000	Ω
t_S	Sampline Time	f_{ADC}=14MHz	0.107	-	17.1	μs
T_{CONV}	Sampling and conversion time	f_{ADC}=14MHz, 12-bit conversion	1	-	18	μs

Table 41 12-bit ADC Accuracy

Symbol	Parameter	Condition	Typical value	Maximum value	Unit
E_T	Total uncorrected error	f_{PCLK}=56MHz, f_{ADC}=14MHz, V_{DDA}=2.4V-3.6V T_A=-40℃~85℃	±2	±5	LSB
E_O	offset error		±1.5	±2.5	
E_G	Gain error		±1.5	±3	
E_D	Differential linear error		±1	±2	
E_L	Integral linearity error		±1.5	±3	

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.11.1.2. Test of Built-in Reference Voltage Characteristics

Table 42 Embedded Reference Voltage Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{REFINT}	Built-in Reference Voltage	-40℃ < TA < +85℃ V_{DD}= 2-3.6 V	1.1882	1.1947	1.2002	V
$T_{S\_vrefint}$	Sampling time of ADC when reading out internal reference voltage	-	-	5.1	17.1	μs
V_{RERINT}	Built-in reference voltage extends to temperature range	V_{DD}=3V ±10mV	-	-	18	mV
T_{coeff}	Temperature coefficient	-	-	-	104	ppm/℃

Note: It is obtained from a comprehensive evaluation and is not tested in production.

5.11.2. DAC

Test parameter description:

- DNL differential non-linear error: the deviation between two consecutive codes is-1 LSB
- INL integral non-linear error: the difference between the measured value at code i and the value at code i on the connection between code 0 and the last code 4095

Table 43 DAC Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{DDA}	Analog power supply voltage	-	2.4	-	3.6	V
R_{LOAD}	Resistive load	Load is connected to VSSA with buffer on	5	-	-	kΩ
R_O	Output impedance	The resistive load between DAC_OUT and VSS is 1.5MΩ with buffer off	-	-	15	kΩ
C_{LOAD}	Capacitive load	Maximum capacitive load at DAC_OUT pin with buffer on	-	-	50	pF

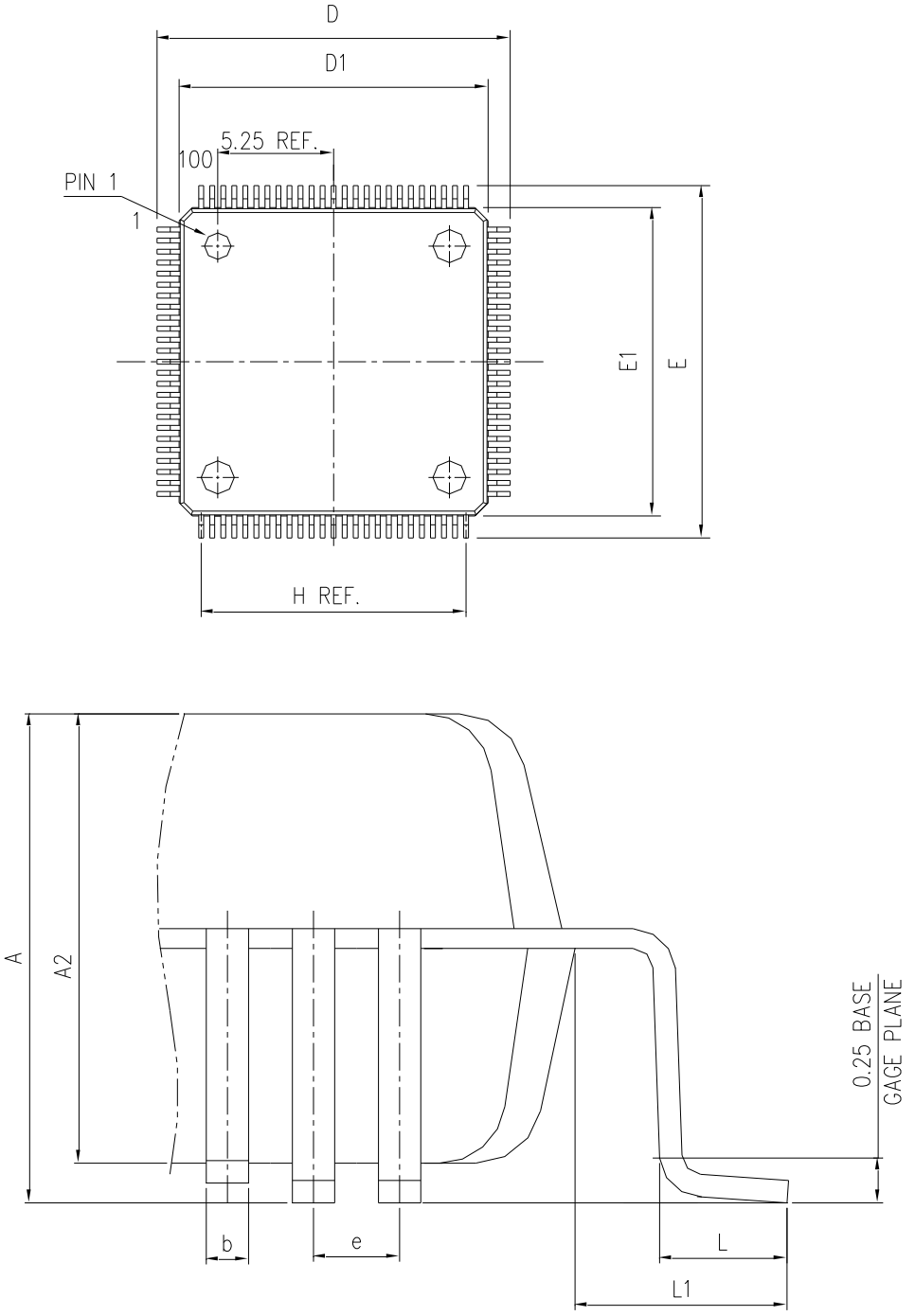
Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
DAC_OUT min	Low DAC_OUT voltage with buffer	Maximum output offset of DAC, (0x0E1) corresponding to 12-bit input code to V_{REF+}= (0xF1B) at 3.6V and V_{REF+}= (0x154) at 2.4V and (0xEAC)	0.39	-	1.94	V
DAC_OUT max	High output voltage with buffer		-10.84	-	4.66	V
DNL	Differential non-linear error	Configured with 12-bit DAC	-1.03	-	0.79	LSB
INL	Integral non-linear error	Configured with 12-bit DAC	-3.86	-	2.46	LSB
Offset	Offset error	V_{REF+}=3.6V, configuring 12-bit DAC	-2.57	-	9.49	LSB
Gain error	Gain error	Configured with 12-bit DAC	-0.0013	-	0.0045	%

Note: It is obtained from a comprehensive evaluation and is not tested in production.

6. Package information

6.1. LQFP100 package diagram

Figure 13 LQFP100 Package Diagram



（1） The figure is not drawn to scale.

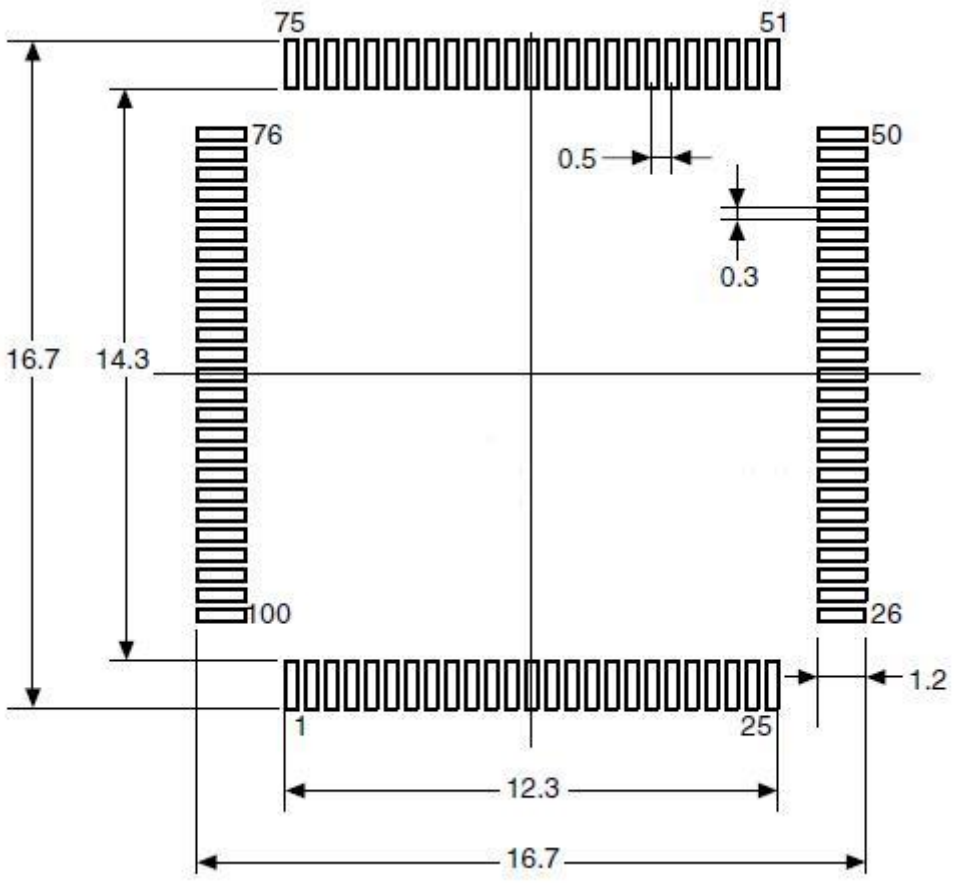
（1） All pins should be soldered to the PCB

Table 44 LQFP100 Package Data

DIMENSION LIST（FOOTPRINT: 2.00）			
S/N	**SYM**	**DIMENSIONS**	**REMARKS**
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	16.000±0.200	LEAD TIP TO TIP
4	D1	14.000±0.100	PKG LENGTH
5	E	16.000±0.200	LEAD TIP TO TIP
6	E1	14.000±0.100	PKG WDTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H（REF）	（12.00）	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

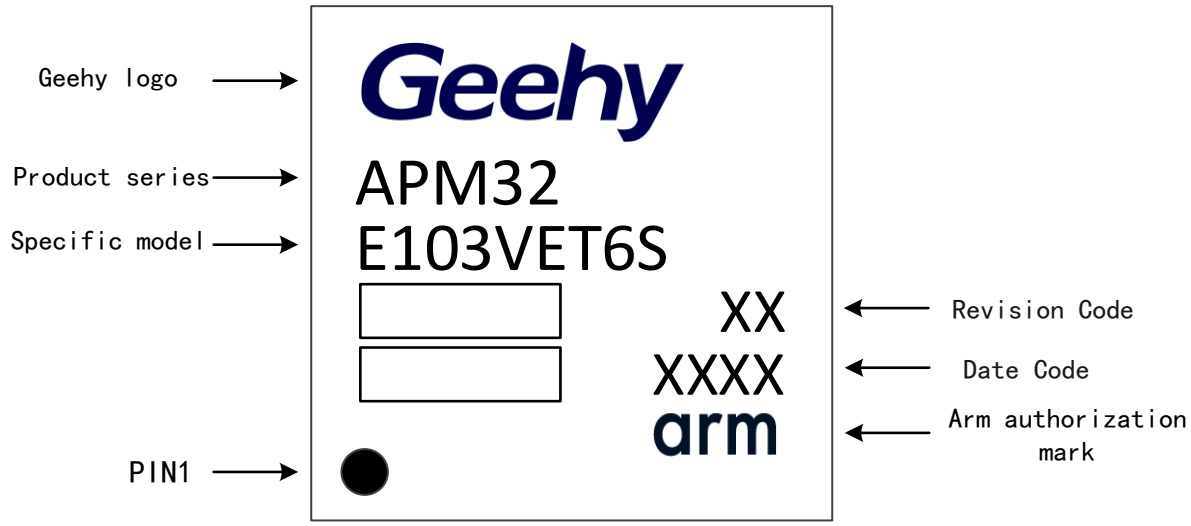
（1） Dimensions are displayed in mm

Figure 14 LQFP100-100 pins, 14×14mm recommended welding Layout



（1） Dimensions are expressed in mm

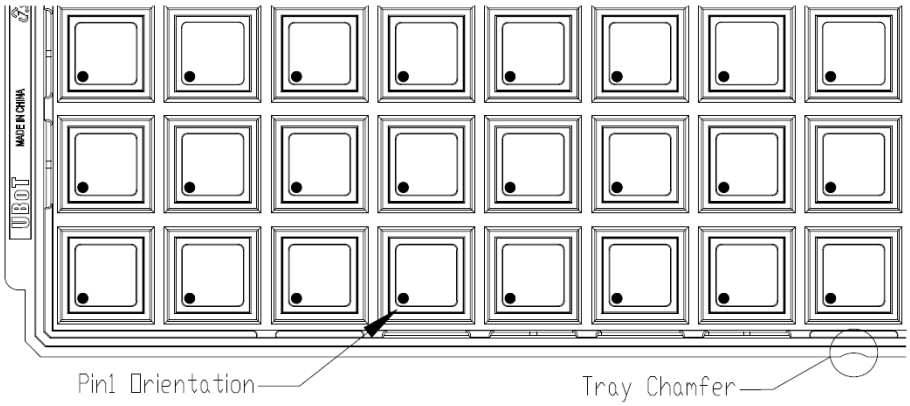
Figure 15LQFP100-100 pins, 14×14mm package identification



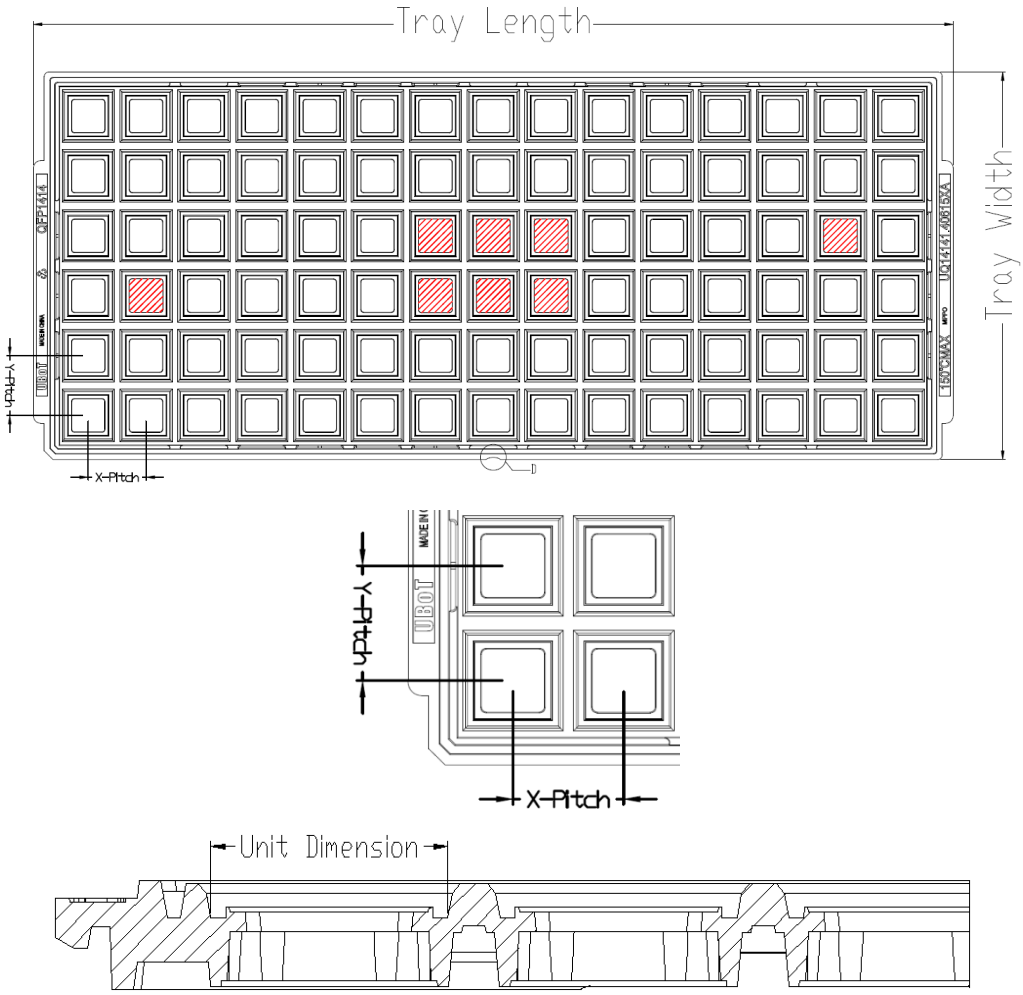
7. Packaging information

7.1. Tray packaging

Figure 16 Tray Packaging Diagram



Tray Dimensions



All photos are for reference only, and the appearance is subject to the product.

Table 45 Tray Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	X-Dimension（mm）	Y-Dimension（mm）	X-Pitch（mm）	Y-Pitch（mm）	Tray Length（mm）	Tray Width（mm）
APM32E103VET6S	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9

8. Ordering information

Figure 17 Product Naming Rules

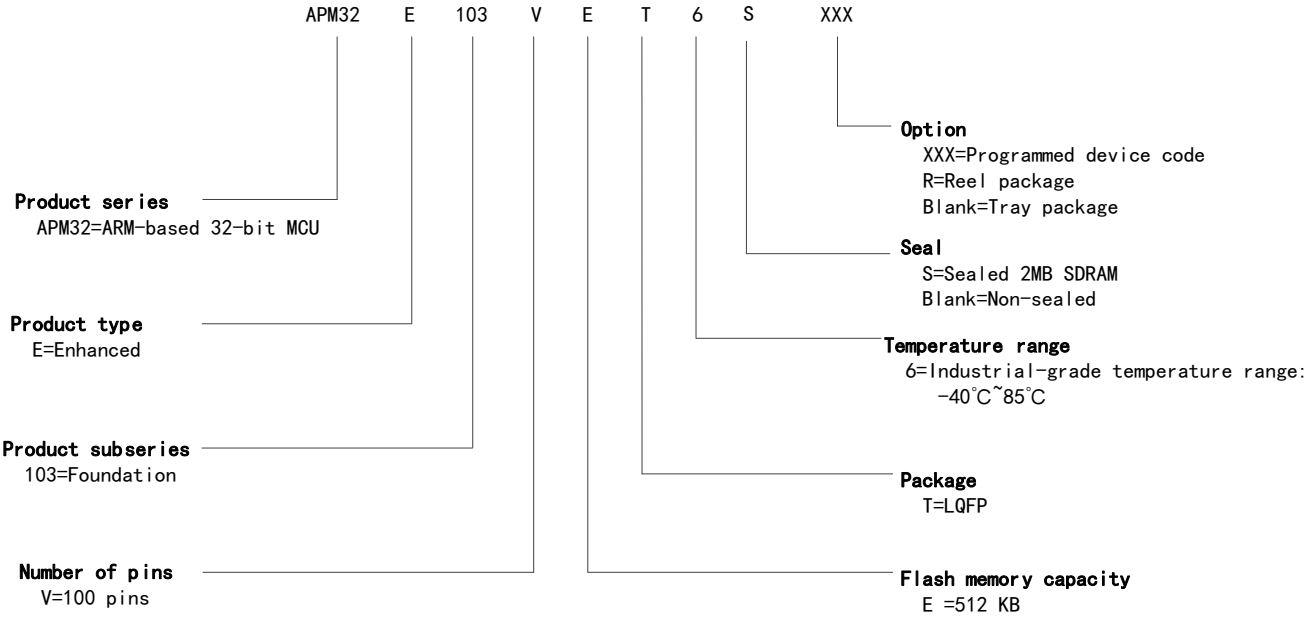


Table 46 Ordering Information Table

Order Code	Flash（KB）	SRAM（KB）	Package	SPQ	Temperature Range
APM32E103VET6S	512	128	LQFP100	900	Industrial grade -40℃~85℃

9. Commonly used function module denomination

Table 47 Commonly Used Function Module Denomination

Chinese description	Short name
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management	RCM
External interrupt	EINT
Genera-purpose IO	GPIO
Multiplexing IO	AFIO
Wake up controller	WUPT
Buzzer	BUZZER
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC controller	CRC
Power Management Unit	PMU
DMA controller	DMA
Analog-to-digital converter	ADC
Real-time clock	RTC
External memory controller	EMMC
Controller local area network	CAN
I2C interface	I2C
Serial peripheral interface	SPI
Universal asynchronous transmitter receiver	UART
Universal synchronous and asynchronous transmitter receiver	USART
Flash interface control unit	FMC

10. Revision History

Table 48 Document Revision History

Date	Version	Change History
January, 2022	1.0	New
June,2022	1.1	(1) Modify Arm trademark (2) Add the statement (3) Modify product naming rules figure
October, 2022	1.2	(1) Modify the frequency range of LSICLK. The minimum is 30 kHz and the maximum is 60 kHz. (2) Modify the accuracy range of HSICLK. The minimum is -1.5% and the maximum is 1.5%.
November, 2023	1.3	(1) Modify the system block diagram, address mapping and pin definition in the table (2) Modify the description of address mapping (3) Modify the ambient temperature to -40~85 ℃ and the junction temperature to -40~105 ℃ (4) Delete the second note under the table of Functions and Peripherals of APM32E103VET6S Chip (5) Modify the table of Power Consumption in Stop Mode and Standby Mode (6) Add SDRAM operating clock instructions
March, 2024	1.4	(1) Modify address mapping of CAN (2) Modify the functional description of CAN (3) Add the note of PB11 pin
June,2025	1.5	(1) Add attention points under general operating conditions (2) Add power-on/power-off characteristics

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8. Scope of Application

The information in this document replaces the information provided in all previous versions of the document.